MDX-65

SERVICE MANUAL

US Model
Canadian Model
AEP Model
UK Model
E Model

Dolby noise reduction extension manufactured under license from Dolby Laboratories Licensing Corporation.
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Model Name Using Similar Mechanism	MDX-62
Mini Disc Mechanism Type	MG-798K-133
Optical Pick-up Name	KMS-241A/J2N

SPECIFICATIONS

System Mini disc digital audio system
Laser Diode Properties
Material: GaAlAs
Wavelength: 780 nm
Emission Duration: Continuous
Laser output Power: Less than 44.6 µW*

* *This output is the value measured at a distance of 200 mm from the objective lens surface on the Optical Pick-up Block.*

Frequency response
10 – 20,000 Hz
Wow and flutter Below measurable limit
Signal-to-noise ratio
95 dB
Outputs Bus control output (8 PIN)
Analog audio output (RCA PIN)
Current drain 300 mA (MD playback)
600 mA (during loading or ejecting a disc)
Dimensions Approx. 176 × 83.5 × 142 mm ($7 \times 3\ ^3/_8 \times 5\ ^{18}/_{32}$ in.) (w/h/d) not incl. projecting parts and controls
Mass Approx. 1.1 kg (2 lb. 7 oz.)
Power requirement
12 V DC car battery (negative ground)
Supplied accessories
Mounting hardware (1 set)
Bus cable 5.5 m (1)
RCA pin cord 5.5 m (1)

- *U.S. and foreign patents licensed from Dolby Laboratories Licensing Corporation.*
- *Design and specifications subject to change without notice.*

FEATURES

- Sony BUS system compatible with **mobile MD changers**.
- **Direct-in system** for inserting and removing MDs easily.
- **No waiting time to change discs** in continuous play.
- The MD changer compartment has a built in light for easy use even in the dark.
- 1 bit Digital/Analog converter for high quality sound reproduction.

MINIDISC CHANGER

MICROFILM

SONY®

SECTION 4
DIAGRAMS

4-1. IC PIN DESCRIPTIONS

• IC100 CXA2523AR (RF AMP)

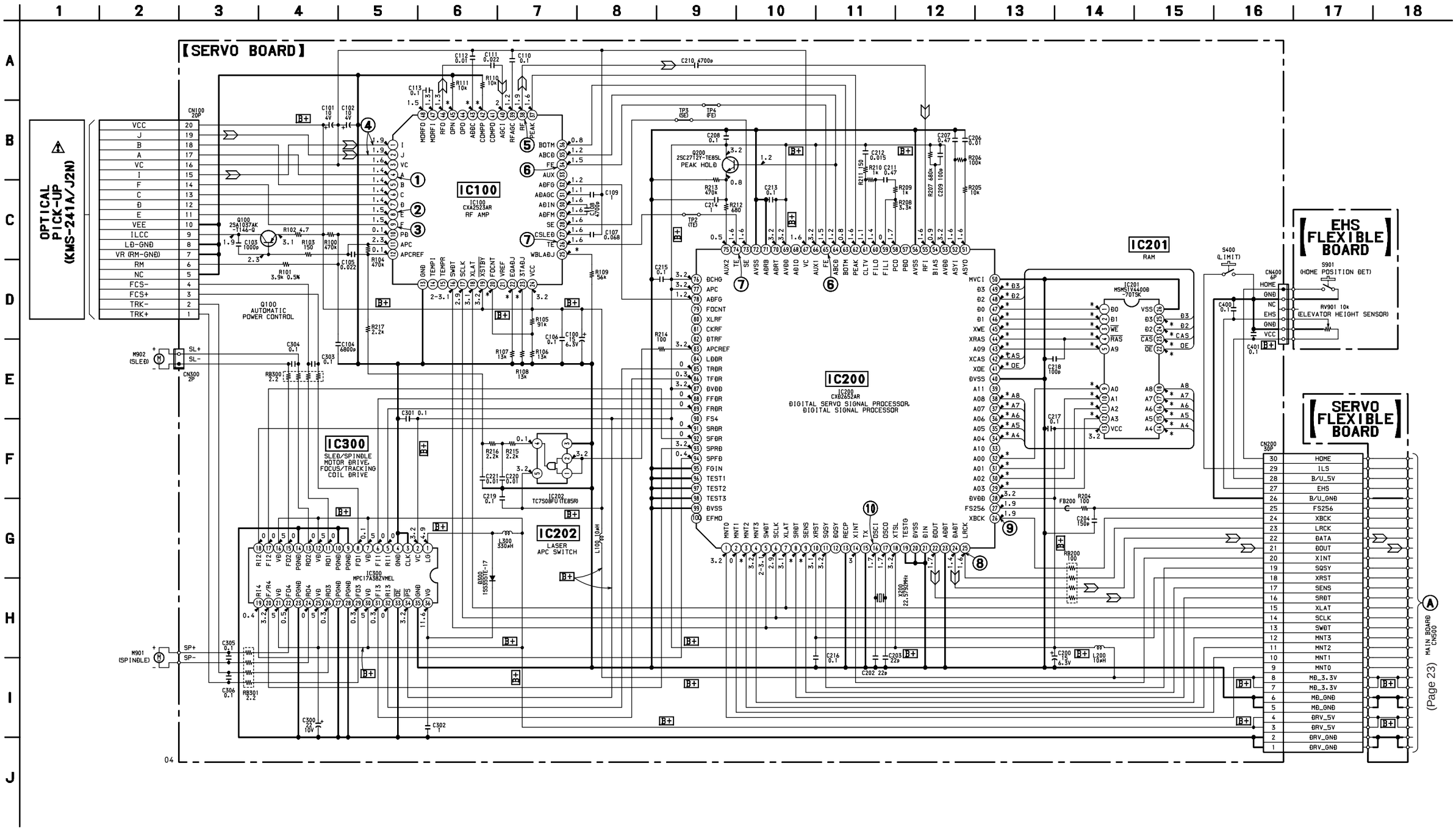
Pin No.	Pin Name	I/O	Pin Description
1	I	I	I-V converted RF signal input (I) from detector of optical pick-up.
2	J	I	I-V converted RF signal input (J) from detector of optical pick-up.
3	VC	O	Center voltage (+1.65 V) generation output
4 – 9	A – F	I	Signal input (A to F) from detector of optical pick-up.
10	PD	I	Quantity monitor input of light from laser diode of optical pick-up.
11	APC	O	Laser amplifier output to automatic power control circuit.
12	APCREF	I	Reference voltage input for laser power setting.
13	GND	—	GND
14	TEMPI	I	Temperature sensor connecting pin (Not used in this set.)
15	TEMPR	O	Reference voltage output for temperature sensor. (Not used in this set.)
16	SWDT	I	Write data signal input from System controller (IC600).
17	SCLK	I	Serial clock signal input from System controller (IC600).
18	XLAT	I	Serial latch signal input from System controller (IC600).
19	XSTBY	I	Standby signal input (“L” : Standby) (Fixed at “H” in this set.)
20	FOCNT	I	Center frequency control voltage input of internal circuit filter (BPF22, BPF3T and EQ).
21	VREF	O	Reference voltage output (Not used in this set.)
22	EQADJ	I	Center frequency setting input of internal circuit filter (EQ).
23	3TADJ	I	Center frequency setting input of internal circuit filter (BPF3T).
24	VCC	—	Power supply pin (+3.3 V)
25	WBLADJ	I	Center frequency setting input of internal circuit filter (BPF22).
26	TE	O	Tracking error signal output to CXD2652AR (IC200).
27	CSLED	I	Connecting pin for low pass filter condenser of sled error signal.
28	SE	O	Sled error signal output to CXD2652AR (IC200).
29	ADFM	O	FM signal output of ADIP.
30	ADIN	I	FM signal input of ADIP by AC combination.
31	ADAGC	I	External condenser connecting pin for AGC of ADIP.
32	ADFG	O	ADIP double FM signal output (22.05 kHz ± 1 kHz) to CXD2652AR (IC200).
33	AUX	O	Support signal (I3 signal/temperature signal) output (Not used in this set.)
34	FE	O	Focus error signal output to CXD2652AR (IC200).
35	ABCD	O	Quantity signal output of light to CXD2652AR (IC200).
36	BOTM	O	Bottom hold signal output of quantity signal (RF/ABCD) of light to CXD2652AR (IC200).
37	PEAK	O	Peak hold signal output of quantity signal (RF/ABCD) of light to CXD2652AR (IC200).
38	RF	O	Playback EFM RF signal output to CXD2652AR (IC200).
39	RFAGC	I	External condenser connecting pin of AGC circuit for RF.
40	AGCI	I	RF signal input by AC combination.
41	COMPO	O	User comparator output pin (Not used in this set.)
42	COMPP	I	User comparator input pin (Fixed at “L” in this set.)
43	ADDC	I	External condenser connecting pin for low frequency interception of ADIP amplifier.
44	OPO	O	External condenser connect pin for lower cut of ADIP amplifier.
45	OPN	I	User operational amplifier inversion input pin (Fixed at “L” in this set.)
46	RFO	O	RF signal output
47	MORFI	I	RF signal input of MO by AC combination.
48	MORFO	O	RF signal output of MO.

• IC600 μPD784216GC-027-8EU (SYSTEM CONTROLLER)

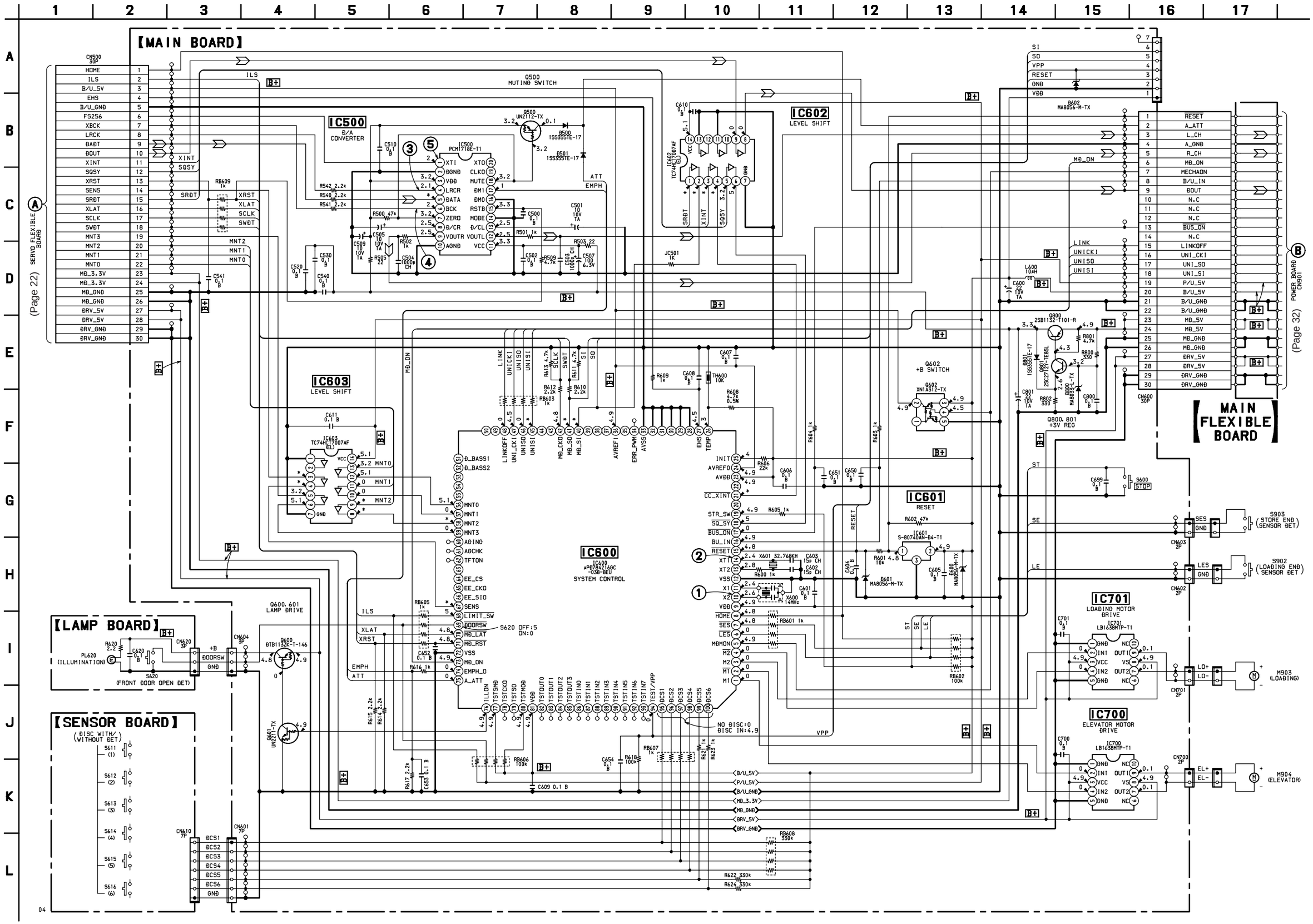
Pin No.	Pin Name	I/O	Pin Description
1	M1	O	Elevator motor (M904) drive signal output
2	$\overline{\text{M1}}$	O	Elevator motor (M904) drive signal output
3	M2	O	Loading motor (M903) drive signal output
4	$\overline{\text{M2}}$	O	Loading motor (M903) drive signal output
5	MDMON	O	Mechanism deck system power control output (“H” : Power ON)
6	$\overline{\text{LES}}$	I	Loading end sensor detection switch (S902) input
7	$\overline{\text{SES}}$	I	Store end sensor detection switch (S903) input
8	$\overline{\text{HOME}}$	I	Home position detection switch (S901) input (“L” : Home position)
9	VDD	—	Power supply pin (+5 V)
10	X2	—	Main system clock connecting pin (14 MHz)
11	X1	—	Main system clock connecting pin (14 MHz)
12	VSS	—	GND
13	XT2	—	Sub system clock connecting pin (32.768 kHz)
14	XT1	—	Sub system clock connecting pin (32.768 kHz)
15	$\overline{\text{RESET}}$	—	System reset input
16	BU IN	I	Backup OFF detection input (“L” : Backup OFF)
17	$\overline{\text{BUS ON}}$	I	BUS OFF detection of SONY BUS. (“H” : BUS OFF)
18	$\overline{\text{SQ SY}}$	I	Sub code Q sync input from CXD2652AR (IC200).
19	STR SW	I	STOP switch (S600) input
20	—	O	Not used.
21	$\overline{\text{CC XINT}}$	I	Interruption status input from CXD2652AR (IC200).
22	—	O	Not used.
23	AVDD	—	Power supply for A/D converter. (+5 V)
24	AVREF0	—	Reference voltage for A/D converter.
25	INIT	I	Initial input pin at reset.
26	TEMP	I	Thermistor connecting pin for temperature detection.
27	EHS	I	Elevator height position detection input
28, 29	—	I	Connect to GND.
30 – 32	—	O	Connect to GND.
33	AVSS	—	Analog GND
34	ERR PWM	O	Error data output (Not used in this set.)
35	—	O	Not used.
36	AVREF1	—	Reference voltage for D/A converter.
37, 38	—	O	Not used.
39	—	—	Not used.
40	MD SI	I	Read data signal input from CXD2652AR (IC200).
41	MD SO	O	Write data signal output to CXA2523AR (IC100) and CXD2652AR (IC200).
42	MD CKO	O	Serial clock signal output to CXA2523AR (IC100) and CXD2652AR (IC200).
43	—	O	Not used.
44	—	—	Not used.
45	UNISI	I	Serial data input for SONY BUS.
46	UNISO	O	Serial data output for SONY BUS.
47	UNI CKI	I	Serial clock input for SONY BUS.
48	LINKOFF	O	Link control signal output for SONY BUS. (“H” : Link OFF)
49	—	O	Not used.
50	—	I	Not used.
51, 52	D-BASS1, 2	O	Digital D-BASS select output 1, 2 (Not used in this set.)
53 – 55	—	O	Not used.
56 – 59	MNT0 – 3	O	Monitor 0 – 3 signal input from CXD2652AR (IC200).
60	AGING	O	Not used.
61	AGCHK	O	Not used.
62	TFTON	O	Not used.

Pin No.	Pin Name	I/O	Pin Description
63	—	O	Not used.
64	EE CS	O	Chip select output to EEPROM. (Not used in this set.)
65	EE CKO	O	Serial clock output to EEPROM. (Not used in this set.)
66	EE SIO	I/O	Data input from/output to EEPROM. (Not used in this set.)
67	SENS	I	Internal status input from CXD2652AR (IC200).
68	$\overline{\text{LIMIT SW}}$	I	Optical pick-up innermost track limit position detection switch (S400) input
69	$\overline{\text{DOORSW}}$	I	Front door open detection switch (S620) input (“L” : Open complete)
70	$\overline{\text{MD LAT}}$	O	Serial latch signal output to CXA2523AR (IC100) and CXD2652AR (IC200).
71	$\overline{\text{MD RST}}$	O	Reset signal output to CXD2652AR (IC200).
72	VSS	—	GND
73	MD ON	O	Servo system power control output (“H” : Power ON)
74	EMPH O	O	De-emphasis circuit control output (“H” : De-emphasis ON)
75	A ATT	I	Analog mute control input (“H” : Mute ON)
76	ILLON	O	Illumination lamp (PL620) light-up control output (“H” : Lamp light-up)
77	TSTSMD	I	Single mode setting pin (“L” : Single mode)
78	TSTCKO	O	Serial clock output to LED for TEST mode display. (Not used in this set.)
79	TSTSO	O	Serial data output to LED for TEST mode display. (Not used in this set.)
80	TSTMOD	I	TEST mode setting pin (“L” : TEST mode)
81	VDD	—	Power supply pin (+5 V)
82 – 85	TSTOUT0 – 3	O	TEST key output pin of 4 × 8 matrix. (Not used in this set.)
86 – 93	TSTIN0 – 7	I	TEST key input pin of 4 × 8 matrix. (Not used in this set.)
94	TEST/VPP	—	Fixed at “L” in this set.
95	DCS1	I	Disc with/without detection 1 switch (S611) input (“H” : with disc)
96	DCS2	I	Disc with/without detection 2 switch (S612) input (“H” : with disc)
97	DCS3	I	Disc with/without detection 3 switch (S613) input (“H” : with disc)
98	DCS4	I	Disc with/without detection 4 switch (S614) input (“H” : with disc)
99	DCS5	I	Disc with/without detection 5 switch (S615) input (“H” : with disc)
100	DCS6	I	Disc with/without detection 6 switch (S616) input (“H” : with disc)

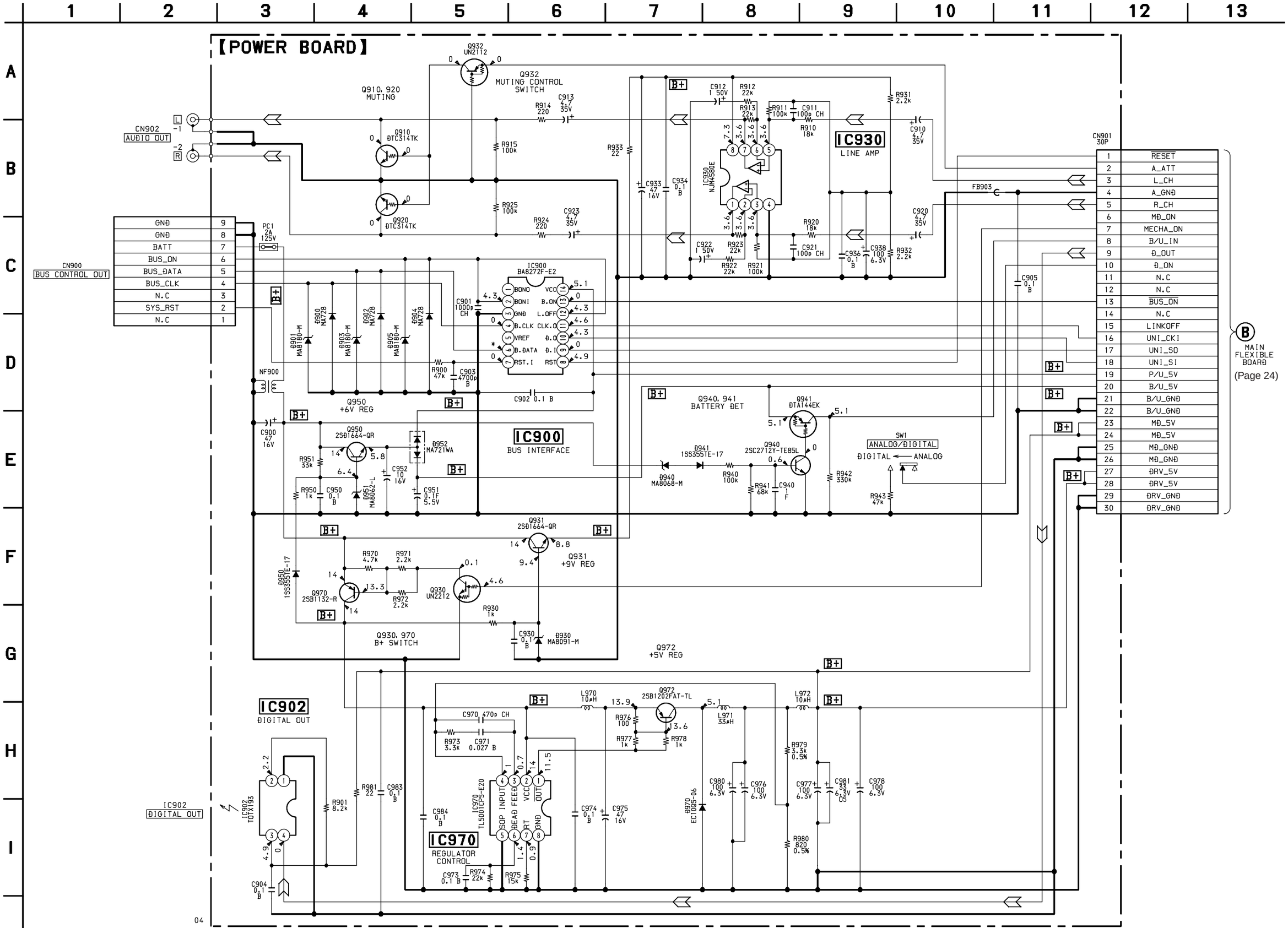
4-5. SCHEMATIC DIAGRAM — SERVO SECTION — • Refer to page 33 for Waveforms and page 35 for IC Block Diagrams.



4-6. SCHEMATIC DIAGRAM — MAIN SECTION — • Refer to page 34 for Waveforms and page 37 for IC Block Diagrams.



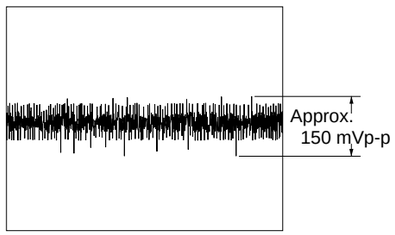
4-9. SCHEMATIC DIAGRAM — POWER SECTION — • Refer to page 37 for IC Block Diagrams.



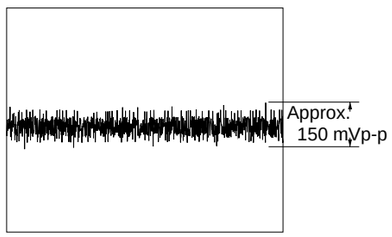
• Waveforms

– Servo Section –

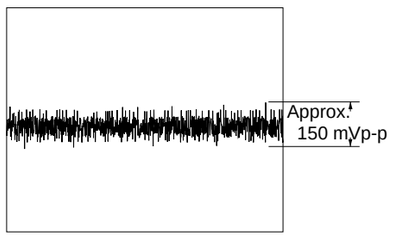
❶ IC100 ④ (A) PLAY MODE
200 mV/DIV, 10 µsec/DIV



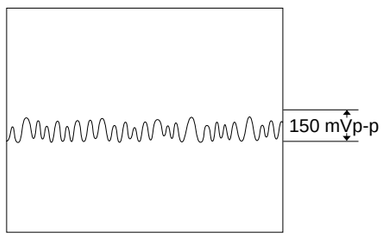
❷ IC100 ⑧ (E) PLAY MODE
100 mV/DIV, 10 µsec/DIV



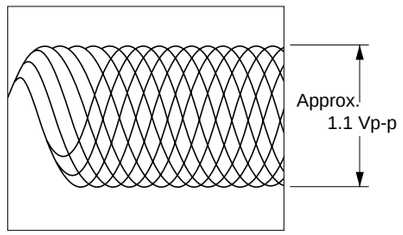
❸ IC100 ⑨ (F) PLAY MODE
100 mV/DIV, 10 µsec/DIV



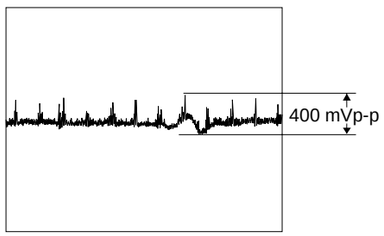
❹ IC100 ①, ② (I, J) PLAY MODE
100 mV/DIV, 10 µsec/DIV



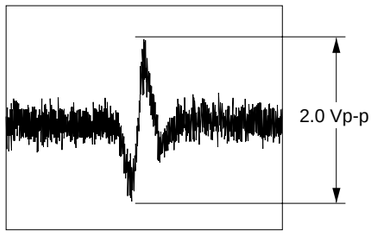
❺ IC100 ㊳ (RF) PLAY MODE
500 mV/DIV, 1 µsec/DIV



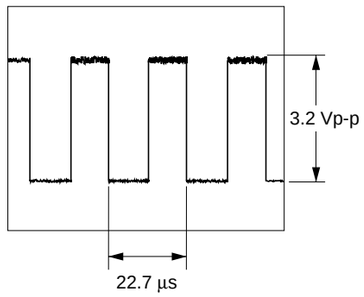
❻ IC100 ㉞, IC200 ⑥ (FE) PLAY MODE
200 mV/DIV, 0.5 msec/DIV



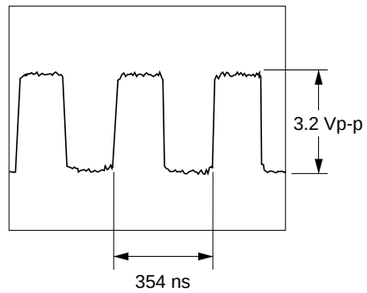
❼ IC100 ㉖, IC200 ㉔ (TE) PLAY MODE
500 mV/DIV, 0.5 msec/DIV



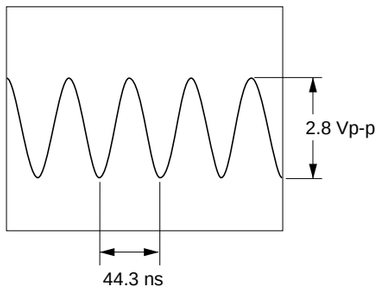
❽ IC200 ㉘ (LRCK)



❾ IC200 ㉖ (XBCK)

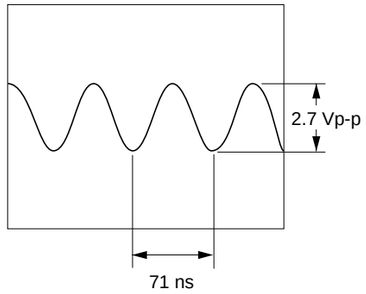


❿ IC200 ⑯ (OSCI)

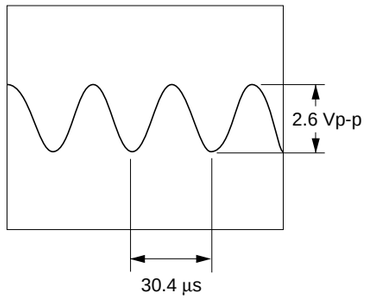


– Main Section –

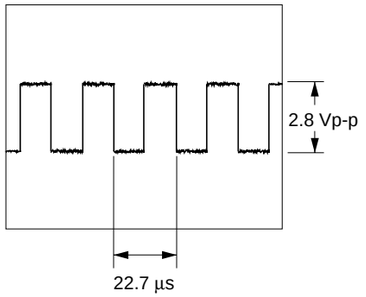
❶ IC600 ⑩ (X2)



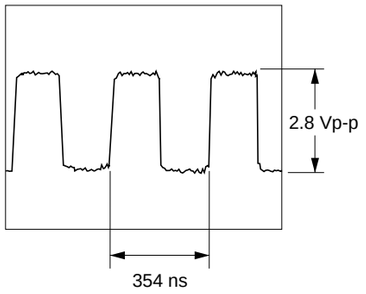
❷ IC600 ⑭ (XT1)



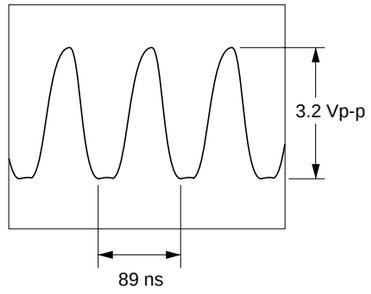
❸ IC500 ④ (LRCK)



❹ IC500 ⑥ (BCK)



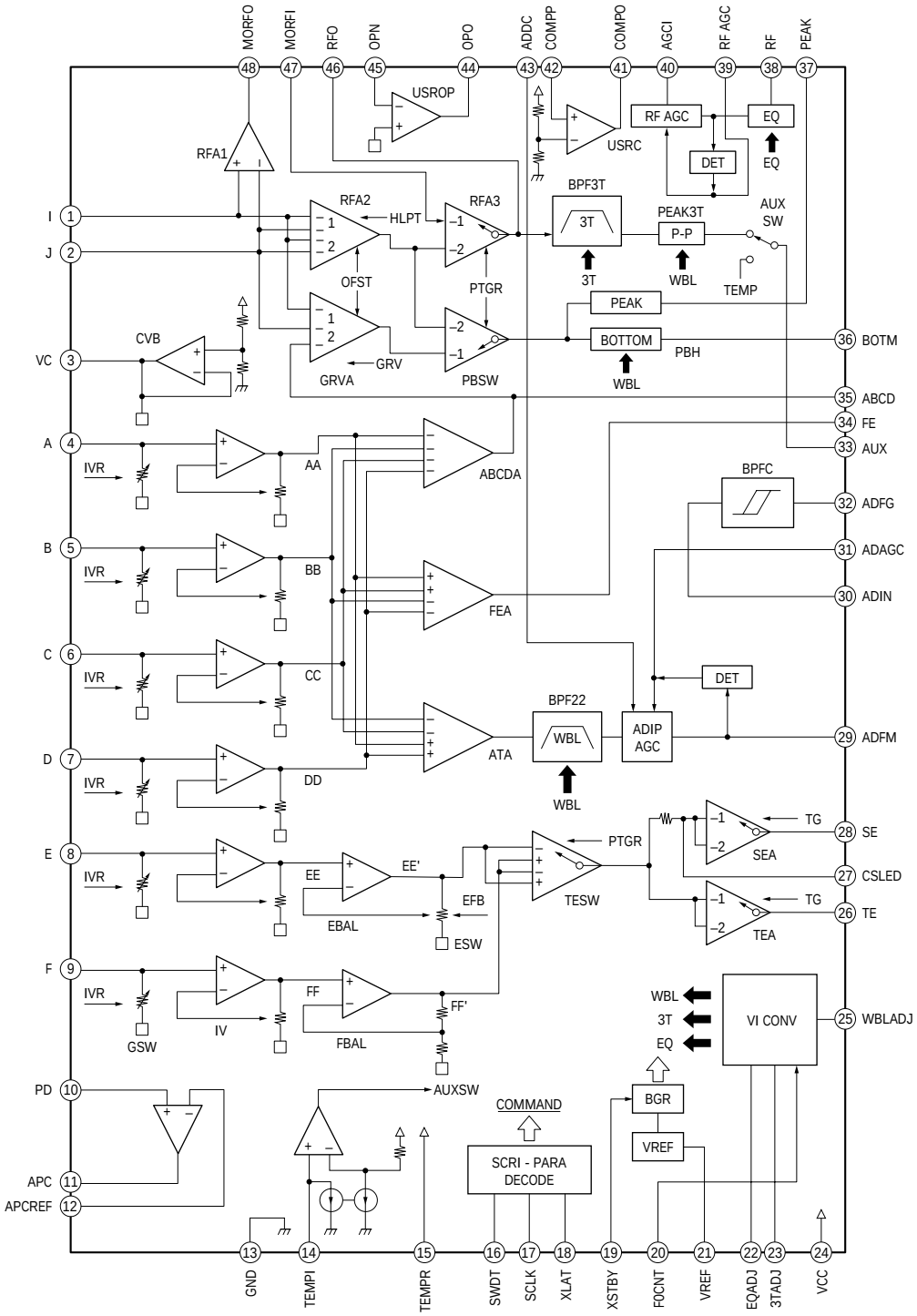
❺ IC500 ① (XT1)



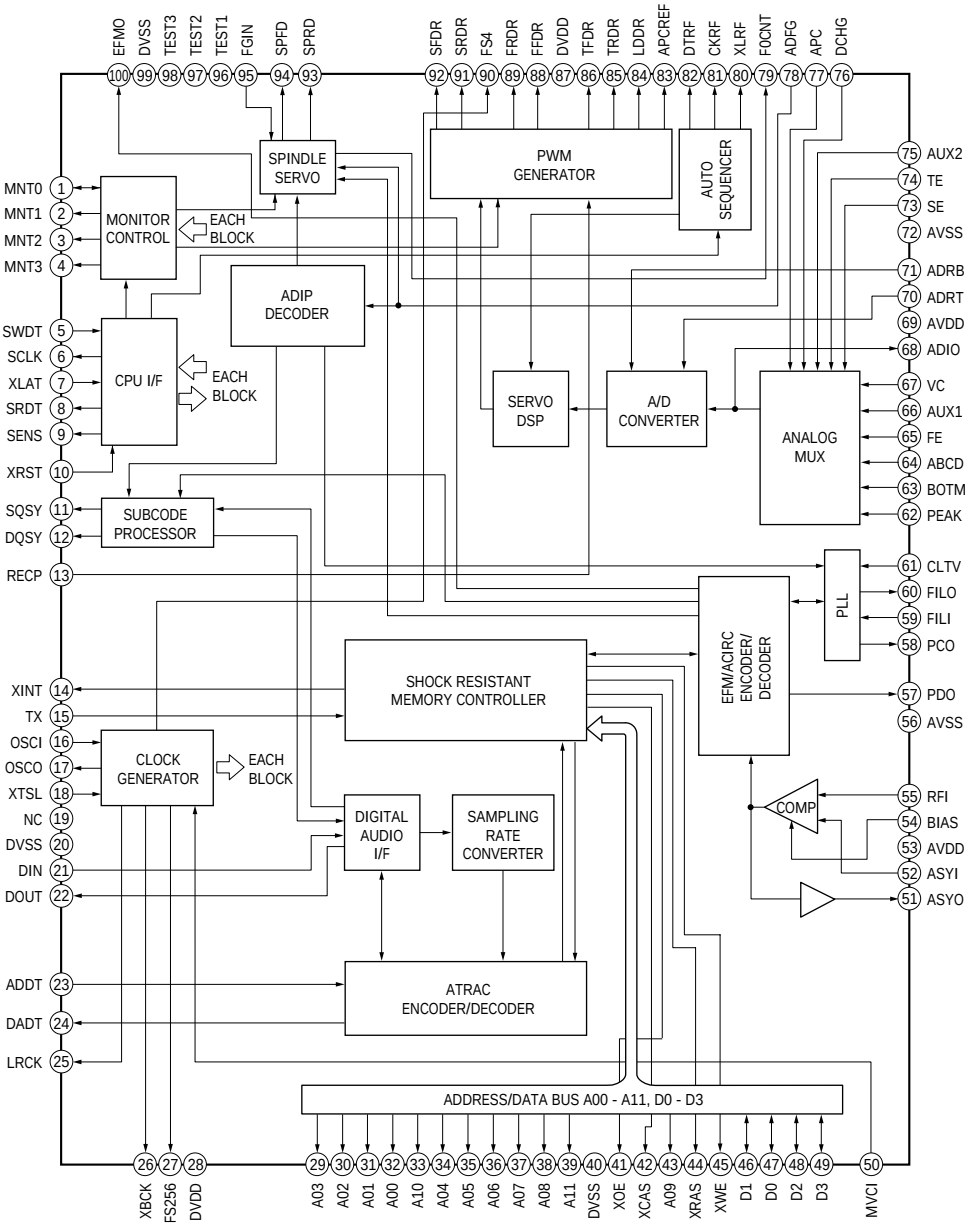
• IC Block Diagrams

– Servo Section –

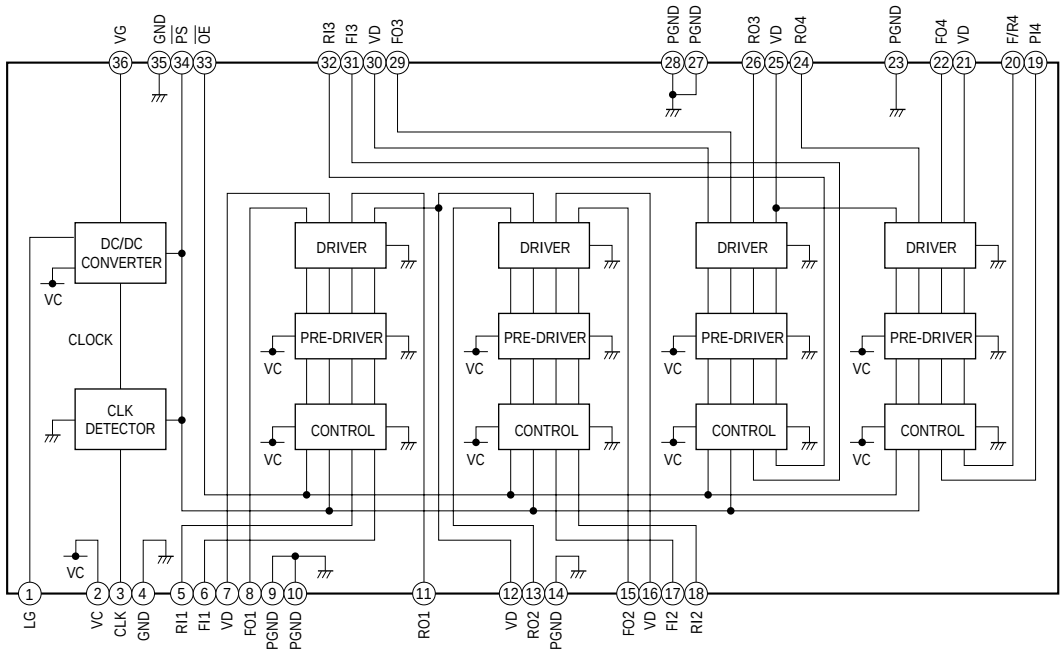
IC100 CXA2523AR



IC200 CXD2652AR

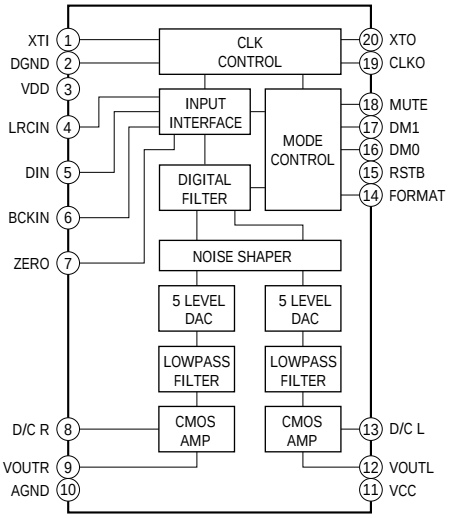


IC300 MPC17A38ZVMEL

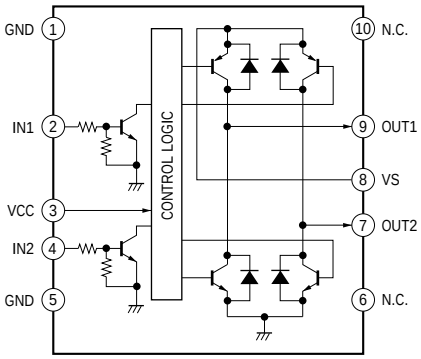


– Main Section –

IC500 PCM1718E-T1

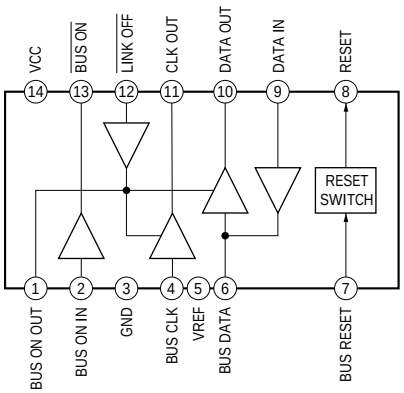


IC700, 701 LB1638MTP-T1



– Power Section –

IC900 BA8272F-E2



IC970 TL5001CPS-E20