NEW TECHNICAL THEORY
FOR SERVICING

CDP-LSA1/MDS-LSA1/STR-LSA1
i. LINK CIRCUIT TROUBLESHOOTING

i. LINK Hi-Fi COMPONENT SYSTEM

SONY

Contents

I. OUTLINE of i. LINK

1. NAME

The IEEE1394, a high speed communication digital interface developed in the PC industry as standard, was standardized by the IEEE (Institute of Electrical and Electronics Engineers). To give this high speed digital serial interface a name which is more familiar than IEEE1394, Sony proposed the name “i.LINK”.
i.LINK is a name of the IEEE1394-1995 and the expansion specifications. It is called “Fire Wire” by Apple Computer in the U.S.

2. CIRCUIT CONFIGURATION

The configuration of the i.LINK circuit can be divided into three layers: PHYSICAL LAYER, LINK LAYER, APPLICATION and TRANSACTION LAYER.

With the IEEE1394, the contents of the PHYSICAL LAYER, LINK LAYER, and TRANSACTION LAYER are defined. The APPLICATION above is defined by the IEC61883 standard for AV equipment, and OHCI (PCI-1394bridge) for PCs, etc.

In the CDP/MDS/STR-LSA1 circuit, the operations are controlled by the three ICs-PHY, LINK, and SYSTEM CONTROL.

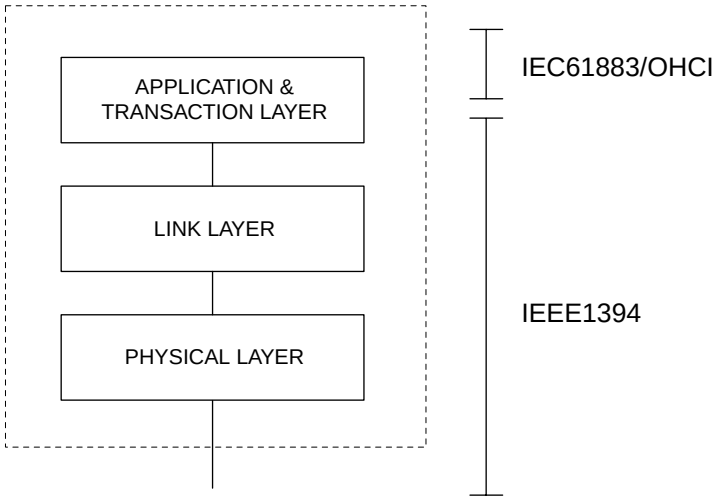


Fig. 1-1. Configuration

(1) PHYSICAL LAYER (PHY)

The i.LINK signals sent between units are H or L digital signals. The PHYSICAL LAYER plays the role of correctly sending this electrical signal output. It is sometimes refereed to as PHY. In the LISSA series i.LINK circuit, operations are controlled by one IC (CXD1945R).

PHY recognizes the input electrical signal as digital signal, and outputs to the LINK LAYER.
It also sends the i.LINK signal (packet data) input to the next device.

If PHY is started, it functions as a repeater which sends the i.LINK signal to other devices. Therefore, there are models which supply power to the PHY even when the power of the unit is OFF so that the function for passing the i.LINK signal is not suspended.

PHY also detects bus resets generated when a new device is connected or disconnected.

(Note) When the power of the PHY is OFF

Some PCs and portable equipment may not supply power to the PHY. Take note that this may not be indicated in instruction manuals.

(2) LINK LAYER (LINK)

Electric signals detected by the PHY are decoded in the logic layer to detect the contents of the signal. This detecting layer is the logic layer. The logic layer is called LINK. In LISSA series i.LINK circuit, one IC (CXD3202AR) controls operations. It also has a PLL circuit to read received audio signals.

In LINK, i.LINK signals are decided to verify the destination sent to and type. If the destination is another device, the contents will be ignored. If the destination is itself or all devices, the type of signal will be verified. If the type can be read by itself, the i.LINK signal is output to the application layer. If the type cannot be read, the application layer is notified that it cannot be read.

If the unit is the ROOT which is the master of the system, the i.LINK sync signal is controlled by LINK. Consequently, power is supplied to LINK like PHY even when the power is OFF.

(3) Application layer

The i.LINK signal output from LINK is received as a command. The layer performing the main operations of the unit is the application layer. The microprocessor controls the operations in the i.LINK circuit of the LISSA series.

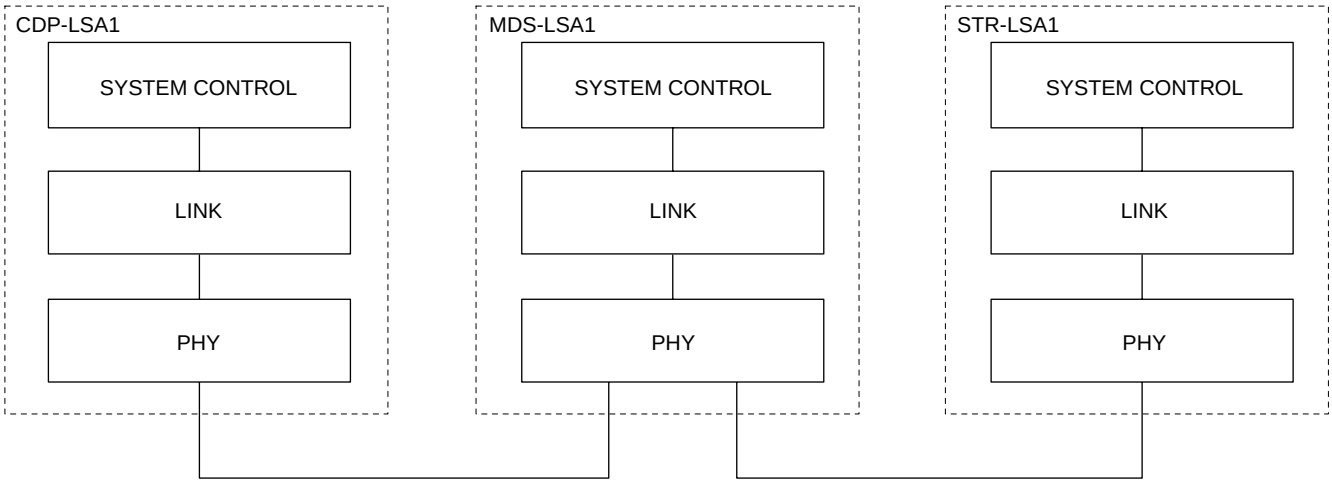


Fig. 1-2. Connection of Unit

3. SYSTEM CONFIGURATION

(1) ROOT

In the i.LINK system connecting the unit by cables, one device is appointed as the ROOT which plays the role of the system manager. ROOT is selected every time a new i.LINK system is configured when the unit is connected or disconnected.

ROOT operates as the system manager of the i.LINK system. When appointed as ROOT, the NODE ID which is the contact number in the current system is set in order from 0 for the other device. The last number (maximum 63) is set as itself.

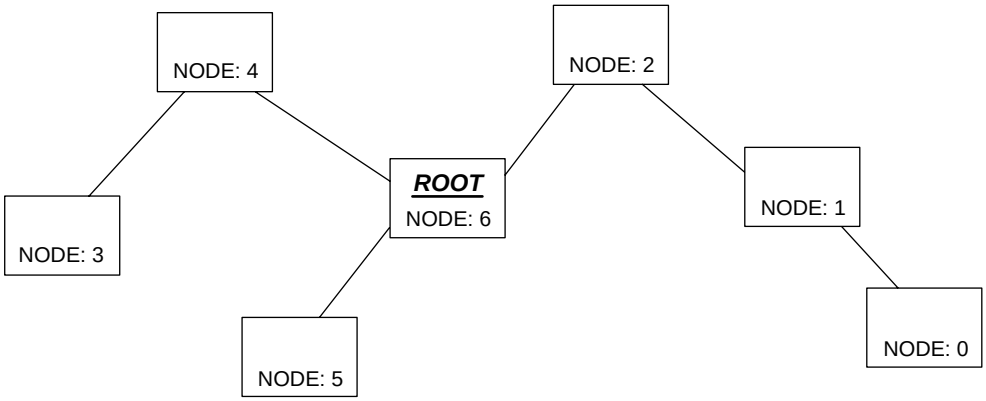


Fig. 1-3. i LINK System

(2) Cycle signal

With the i.LINK system, periodical (every 8 kHz, 125 µs) sync signals are generated and managed in time division so that the communication is not interrupted. The cycle signal (8 kHz) ROOT is output every 125 µs. Each device synchronizes with this signal and declares the start of communication.

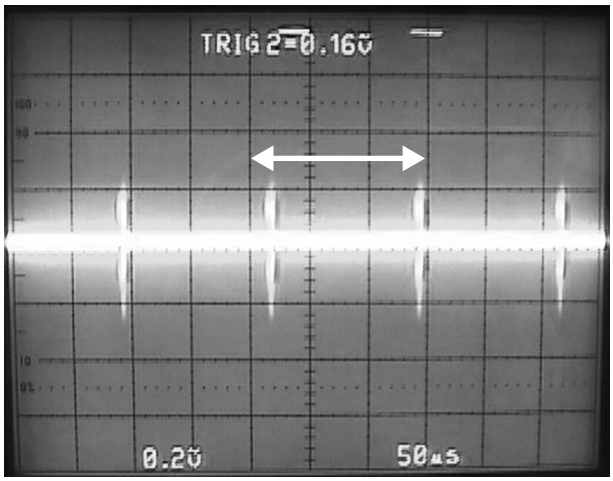


Fig. 1-4. Cycle Signal

As the i.LINK system corresponds to plug-in and plug-out, this sync timing is used to detect the connection and disconnection of new devices to or from the i.LINK system.

(3) Transmission and reception of data

As the i.LINK signals input to a certain device is output directly to the next device, the i.LINK signals are shared by all devices. This means that the communication data specific devices are also all input to other devices.

With the i.LINK system, data by packet is attached with an address and sent. The packet data is sent to all devices and decided by the device data corresponding to the address. NODE ID is used for the data address, but it is also possible to output the data without specifying the address (Broadcast output).

(4) Data transmission speed

The i.LINK devices has three communication speeds-100, 200, and 400 Mbps. They are called S100, S200, and S400. The devices with fast communication speed enable to communicate with slow devices. Consequently, the S400 device is able to handle three communication speeds of S100, S200, and S400. On the other hand, S100 devices are unable to receive nor send S200 and S400 signals.

In the communication between devices, the packet data can be output according to devices with the slowest maximum transfer speed. Therefore data communication is performed at the S100 speed during communication between S400 and S100.

(NOTE) Cable transfer speed restrictions

The maximum transfer speed of the i.LINK cable differs according to the cable type. With the S100 cable, the S200 and S400 signals cannot be sent nor received. As the DV cable is a S100, be careful not to use it incorrectly.

If a cable with low maximum transfer speed is used incorrectly, the communication signal will deteriorate, resulting in improper transmission and reception, and incorrect operation of the unit.

(NOTE) i.LINK device data transfer restrictions

In the communication of i.LINK devices, the maximum transfer speed is checked mutually, and data is transferred at the appropriate speed. If devices that are incompatible with this speed exist on the data transmission path, data may not be transferred correctly. When connecting i.LINK, make sure there are no devices with low transfer speed on the transmission path.

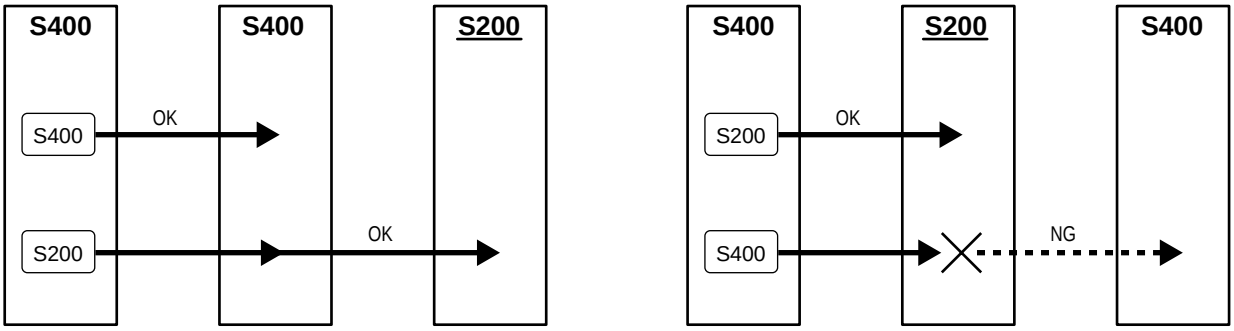


Fig. 1-5. Connection of Devices

(5) Data type

Packet data communicated between devices consist of “Isochronous packet” with time restrictions in transmission and the “Asynchronous packet” with no restrictions.

With the isochronous packet, data transmission is guaranteed to complete with every cycle signal. If the signal does not arrive within a certain period of time, images and sounds will be interrupted. The data will not be resent even if communication error occurs.

The asynchronous packet is data such as commands, and is output while the isochronous packet is not sent. Since time restrictions are lax, data can be resent when errors occur.

(Reference) Capacity of isochronous packet (Band width)

When sending video and audio signals (isochronous packet) simultaneously, signals exceeding bus capacity (100/200/400 Mbps) cannot be sent. If the total capacity exceeds the bus capacity, the device displays an error message (Bus Full) and additional communication will not be possible.

For example, when attempts are made to link to other devices from the STR-LSAI, if the band is full and no new links are possible, the STR-LSAI displays “Bus Full”. In this case, the LINC of this STR-LSAI will not be established, but the existing LINCs will be preserved as they are.

When the device sends signals by S100, the band in which the isochronous signal can be used with S100 is Approx. 80 Mbps. With S100, the images of the DV device is about 35 Mbps while MPEG signals such as TV are 30 to 40 Mbps (Max. about 60 Mbps). The audio signal is about 12 Mbps during high speed dubbing and about 3 Mbps during normal playback. However, when signals are sent by S200/S400, the transfer speed will be about 2 times or 4 times.

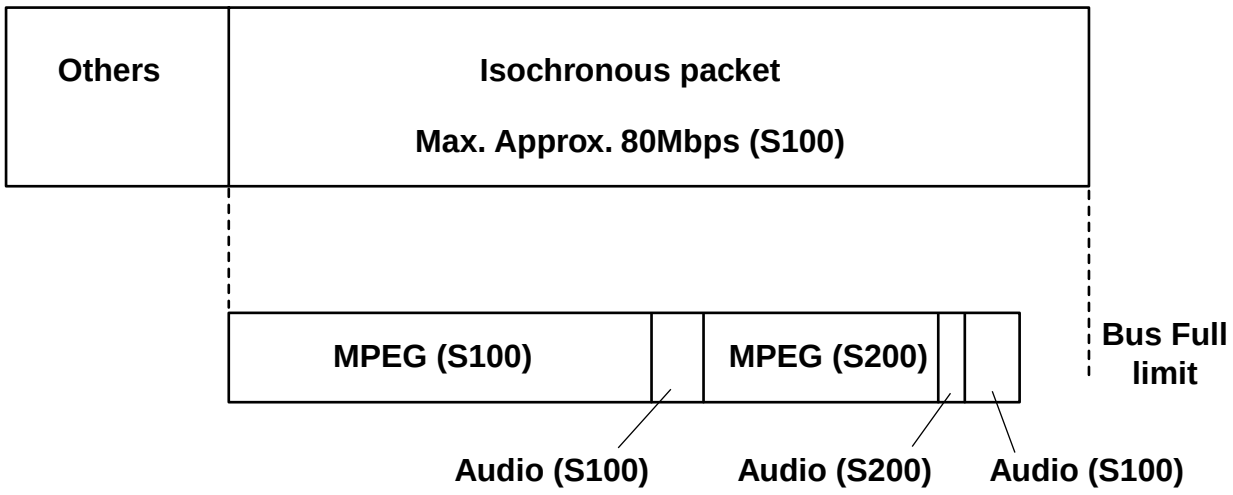
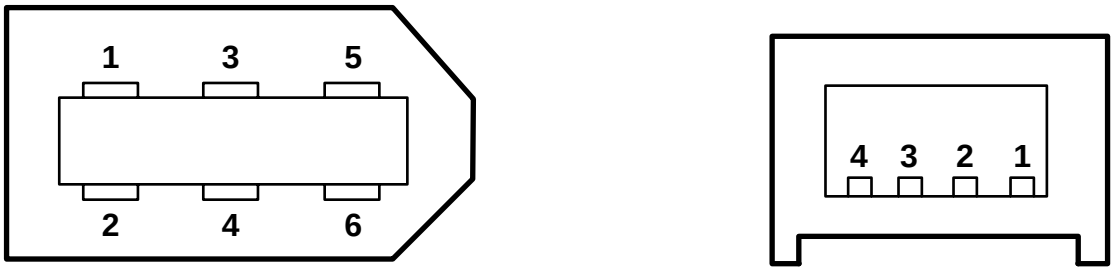


Fig. 1-6. Capacity of Isochronous Packet

4. SYSTEM OPERATIONS

(1) Signal Terminal

There are two types of i.LINK terminals -Pin 6 and Pin 4. The Pin 6 has four signal lines and two power supplies. The Pin 4 has four signal lines. The signal lines are paired. Two are for out and two for input. The i.LINK signal is sent as the differential voltage of the two lines.



1: VP	4: TPB
2: VG	5: TPA*
3: TPB*	6: TPA

1: TPB*	3: TPA*
2: TPB	4: TPA

Fig. 1-7. Signal Terminals (Plug Side)

(2) Cable Bias Voltage

The two output pins is always output with approximately 1.85 V DC voltage (cable bias). The cable bias voltage output from the unit is monitored by the output destination device and detects the connection/disconnection of the device.

In the same way, the two terminals for input monitor the cable bias voltage output from the adjoining devices to detect the connection and disconnection of adjoining devices.

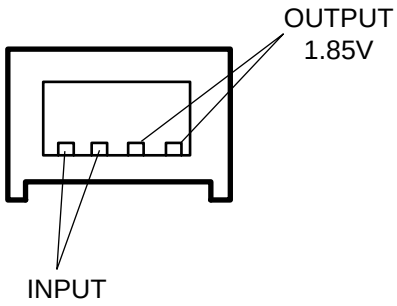


Fig. 1-8. i.LINK Terminal Voltage (Jack Side)

(3) Bus Reset

When a different device is connected to or disconnected from the i.LINK device, the changes in the i.LINK system are detected to generate bus reset. Bus reset detects the connection or disconnection of cables from the cable bias voltage input from the connected device.

When bus reset occurs, the i.LINK system is restructured by the following process.

- Output of bus reset signal (approximately 170 µs)
- Determination of ROOT
- Resetting of node number

1. Output of bus reset signal

The device detecting the connection or disconnection of a new device outputs the bus reset signal (approximately 170 µs) to all devices. This starts the initialization of the bus.

2. Determination of ROOT

The ROOT device is determined in the i.LINK system. Some devices are more inclined to being set as the root according to the applications of the device.

(Note) LOOP Connection

If set to loop connection, errors will occur in the process to determine the root, resulting in timeover. For this reason, by determining the timeover in the process of determining the root, loop connection is detected. If it cannot be determined correctly, errors occur in the operations of the unit. (NO SIGNAL is displayed, etc.)

3. Re-setting the node number

When the root has been determined, the node number is re-set from 0. The node number is used as the destination of the communication between devices. The last maximum value is the node number of ROOT. (Maximum is 63)

(Repair Tips) When “NEW CONNECT” is displayed

When bus reset occurs, “NEW CONNECT” blinks with the LISSA series devices. To check for contact defects of cables and connectors, move the cables or connectors after connecting the unit, and check if bus reset occurs.

(Reference) Bus reset during recording

If bus reset occurs while transmitting music data, the sound skipping may happens. If recording on a MD player, do not connect/disconnect the i.LINK cable of any device.

(Reference) Disconnecting the i.LINK cable

If the cable itself disconnects while connecting, bus reset will occur at one side, and normal operations will be performed at the opposite side, and bus reset will occur continuously. In this case, the application will hang up, or continuous bus reset will be detected, resulting in error messages, etc.

(4) LINC

With the i.LINK system, there are 64 lines (0 to 63) for sending video and sounds between devices. These lines reserve ROOT when it is being used between devices, set it so that it cannot be used by other devices. This method is called P to P (Point to Point) connection for one device to communicate with another device. The LINC (Logical INterface Connection) described in the instruction manual corresponds to this P to P connection.

(Reference) Transmission in no-LINC state (Broadcast communication)

Sending data in the no-LINC state is called Broadcast communication. In Sony DV camcorders, the 63rd channel of the transfer line is used for outputting signals of the DV camcorder.

Even when audio signals are output in the no-LINC state in Sony audio devices, broadcast communication will be performed. (Example: STR-LSA1 Tuner output, etc.)

When sending music data with the input device selected amongst LISSA series devices and LISSA series devices, the data will always be LINCed and output. However, when not LINCed from other devices, the audio signals will be broadcast-output.

(Note) Simultaneous use of channels

Only one signal can be used by channels. When two DV camcorders are set to the playback state and broadcast communication is performed, the signal which started playback later will dominate the channel.

(Reference) Devices performing broadcast communication

When LISSA series devices which are not LINCed with other devices start playback, the signals of the DV camcorder will be blocked by LISSA series' signal. In this case, the DV camcorder will be stopped once, and when playback is started again, the 63 channel will be dominated by DV camcorder again.

(5) i.LINK signals

i.LINK signals consist of the cable bias voltage, cycle signal, i.LINK header signal, and i.LINK data signal.

① Connection with other devices

With the LISSA series, if other devices are not connected, only the cable bias voltage will be output.
When the cable bias of other devices are detected by the i.LINK terminal, the cycle signal which is a sync signal will be output.

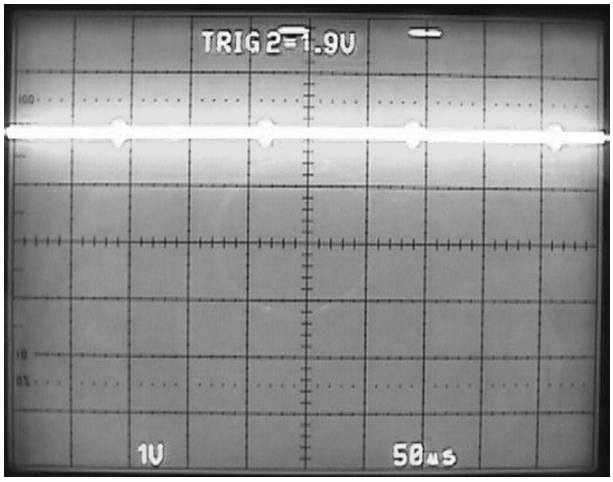
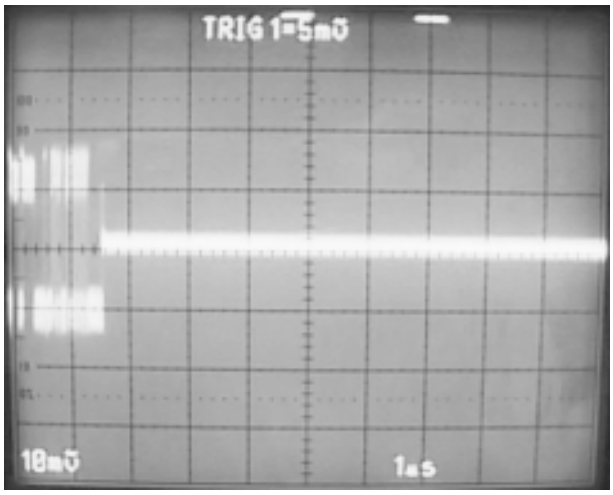


Fig. 1-9. Output of Cycle Signal

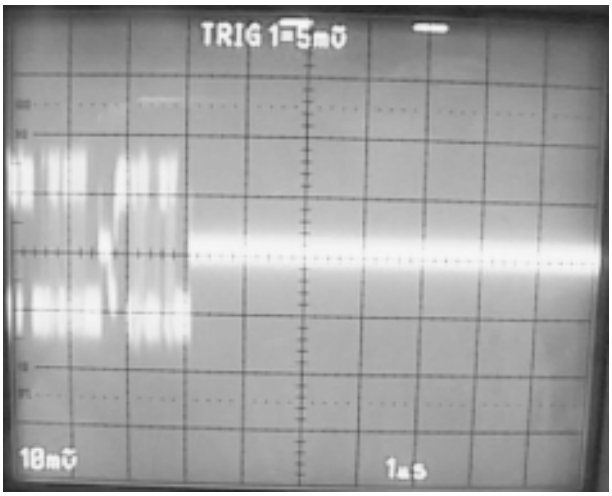
② LINC

When the input destination is LINCed with other devices, the i.LINK header signal will be output after the cycle signal. When devices which cannot be LINCed (incompatible PC, etc.) are selected as the input destination, only the cycle signal will be output.

As the i.LINK data signal is smaller than the cable bias voltage, the oscilloscope is checked in the AC mode (10 mV, 1 µs).



Before LINC
(Only cycle signal)



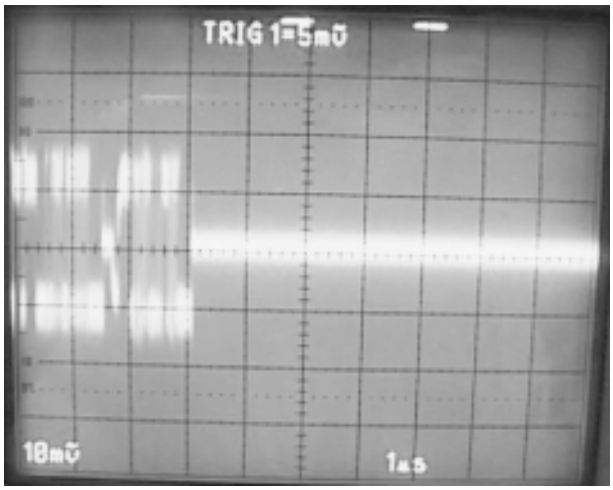
After LINC
(Cycle signal+ header signal)

Fig. 1-10. Output during LINC

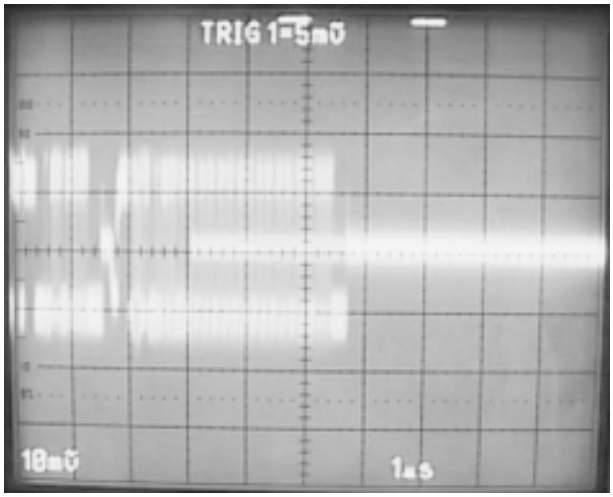
③ Music playback

When data is communicated between LINCed devices, the i.LINK data signal will be output. As the header signal and data signal are an isochronous packet with no time-related transmission restrictions, they are given priority than the asynchronous packet with no time-related restrictions, and sent immediately after the cycle signal.

i.LINK signals such as video and audio signals are composed of the header signal and data signal. When sending music data between LINCed LISSA series devices, data will be sent at 200 Mbps.



Before music playback
(Cycle signal + header signal)



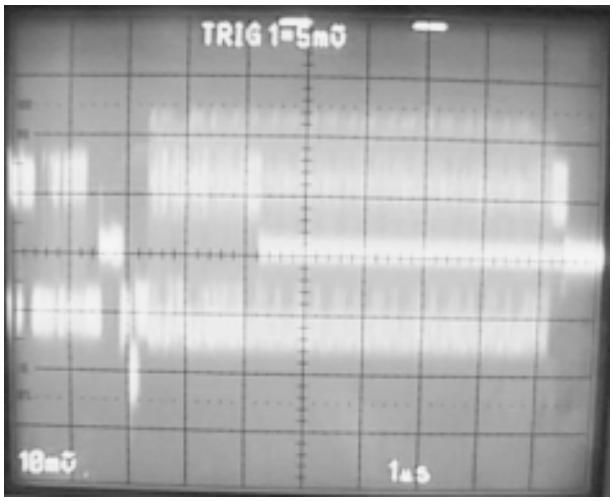
During music playback
(Cycle signal + header signal + data signal)

Fig. 1-11. Output during Music Playback

(Note) i.LINK output of STR-LSA1

When TUNER or ANALOG is selected by switching the input source of the STR-LSA1, music data will be output in the non-LINC state (broadcast output). When a LISSA series device broadcast outputs data, data will be sent at 100 Mbps instead of 200 Mbps. For this reason, the signal waveform on the display of Oscilloscope will be longer along the time axis during LINC playback.

(Refer to Fig. 1-11 and Fig. 1-12)



During music output
(Cycle signal + header signal + data signal)

Fig. 1-12. Waveform during Music Output at 100 Mbps

II. CIRCUIT OPERATIONS

1. POWER SUPPLY CIRCUIT

(1) Starting PHY and LINK

3.3 V drive voltage (3.5 V for MDS-LSA1 only) is supplied to PHY and LINK from the power supply circuit. PHY starts up when voltage is supplied to the LPS terminal (Pin 5), while LINK starts when reset is cleared by the H input to the RESET terminal (Pin 85).

(2) Output of cable bias voltage (PHY)

When PHY starts, cable bias voltage (1.85 V) is output from the TBIAS2/TBIAS0 terminal (Pins 46/48). The cable bias voltage is output to TA2N /TA2P/TA0N/TA0P terminals via the buffer (transistor). When the AC power is turned ON/OFF, the transistor goes OFF by the signal output from the microprocessor, and cable bias is muted to prevent PHY mis-operations.

2. CLOCK CIRCUIT

(1) Master clock (PHY, LINK)

The master clock of the i.LINK operation circuit is the 24.576 MHz of the crystal oscillator connector to the XO/XI terminal of PHY (Pin 32/33). This clock is divided by 1/2 by PHY, and output to the SYSCLK terminal (Pin 83) of LINK from the SCLK terminal (Pin 8) of PHY.

If PHY and LINK are not started, check the master clock input.

(2) Cycle signal (PHY)

When an external device is connected, and the cable bias voltage is output from the external device to the i.LINK terminal, it is detected by the TA2N/TA2P/TA0N/TA0P terminals (Pins 51/52/59/60) of PHY, and PHY performs bus reset operations. When an external device is detected, and the ROOT device is determined by the i.LINK system, the cycle signal (8 kHz/125 µs) which is the sync signal of i.LINK will be output from ROOT.

When the unit is the ROOT, the cycle signal is generated inside PHY, and output from the TA2N/TA2P/TA0N/TA0P terminals (Pins 51/52/59/60).

(Note) When no cycle signal is output

When other devices are not detected, the cycle signal will not be output. Consequently, it will not be output if other devices are not connected to the unit or when a VAIO PC which has not been turned ON is connected.

3. SIGNAL CIRCUIT

(1) i.LINK signal input (PHY)

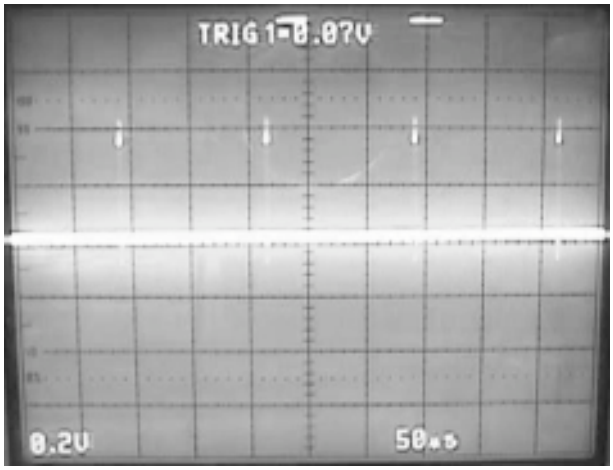
The i.LINK signal input from other devices are input as the TB2N and TB2P signals of the i.LINK terminal, or the differential signal of the TB0N and TB0P. These signals become inversed waveforms.

(2) Communication of PHY and LINK

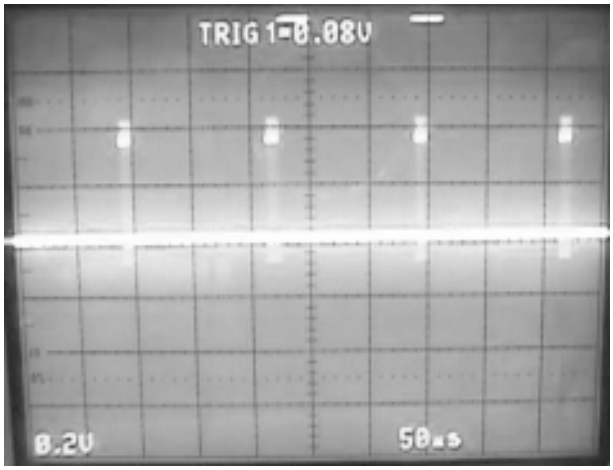
Packet data is extracted from the input i.LINK signal inside the PHY, and output from the DATA0 to 3 terminals (Pins 13/14/16/17) to LINK. At this time, the control signal of mutual communication is output or input from or to the CTL0/CTL1 terminal (Pin 10/11) of PHY.

(Repair Tips)

When other devices are detected by the i.LINK terminal, signals will be output to the DATA0 to 3 terminals of PHY and LINK and CTL0/1 terminal. If no signal is output to these terminals, check the clock input, power line, etc.

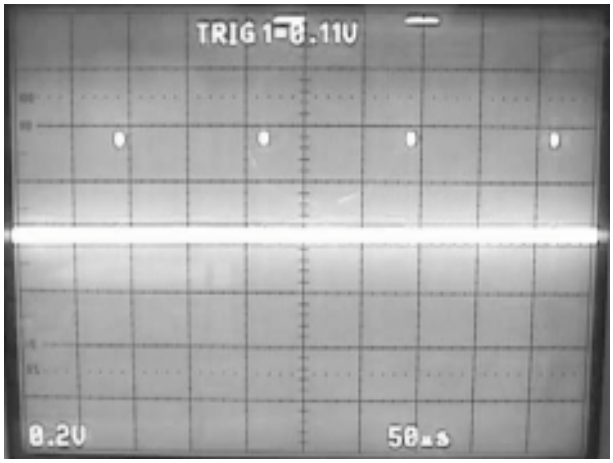


When stopped

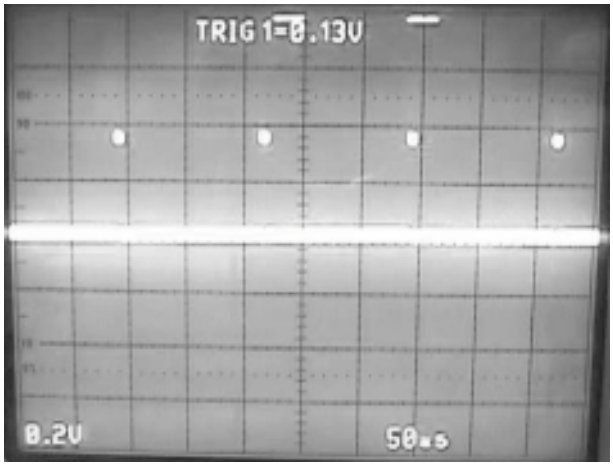


During playback

D3 terminal (LINK Pin 74)...2 V/div, 50 µs



When stopped



During playback

CTL0 terminal (LINK, Pin 80)...2 V/div, 50 µs

Fig. 2-1. Signals between PHY-LINK

(3) Packet data (LINK)

The handling of packet data input to LINK differs according to the data type. The data type of the packet data input is checked. If it is music data which can be played back, it is sent to the playback circuit. If the data cannot be played back (for image, etc.), it will be ignored. If it is self-addressed command data (LINC request, etc.), it will be transferred to the microprocessor.

(4) Communication between LINK and microprocessor

When the i.LINK circuit connected to the AC power supply is started, communication will constantly be performed with the microprocessor using the 16 DATA terminals (Pins 38 to 54) of LINK, eight address terminals (Pins 63 to 70), and four control terminals (Pins 57, 58, 59, and 61).

(5) Communication with playback circuit (LINK)

When LINK receives music data which can be played back, it outputs the data to each playback circuit. On the other hand, if music data is sent to LINK from the playback circuit, it is converted to packet data inside LINK.

① CDP-LSA1

Input of audio data from CD circuit
- Audio data: DATA1 terminal (Pin 15)
- Signal clock: BCKI terminal (Pin 13), LRCKI (Pin 14) terminals
- Subcode signal: ABSO terminal (Pin 101)
- Clock of subcode signal: EXCK terminal (Pin 102), WFCK terminal (Pin 103)
- Error status during CD playback: C2PO terminal (Pin 100)

② MDS-LSA1

Input of audio data from MD circuit
- Audio data: DATAI terminal (Pin 15)
- Signal clock: BCKI terminal (Pin 13), LRCKI terminal (Pin 14)
- Subcode signal: SQSY terminal (Pin 99)
- For high speed downloading of ATRAC data: 512FSIN (Pin 2)...preliminary circuit/ Currently not used

Output of audio data to MD circuit
- Audio data: DATAO terminal (Pin 22)
- Signal clock: BCKO terminal (Pin 20), LRCKO terminal (Pin 21)

③ STR-LSA1

When the H.A.T.S. circuit is ON, the music signal is stored once in the DRAM, synchronized to internal clock of the unit, read from the DRAM, and output to the STR circuit. When the H.A.T.S. circuit is OFF, it will be output to the STR circuit immediately.

Audio data input from the STR circuit
- Audio data: DIN terminal (Pin 17)

Audio data output to the STR circuit (When H.A.T.S. is OFF)
- Audio data: DOUT terminal (Pin 18)
- For error flag waveform shaping: EOF terminal (Pin 23)

Audio data input/output with DRAM (When H.A.T.S. is ON)
- Audio data: DATA terminal (Pins 127 to 143)
- Address signal: Terminal A (Pins 111 to 121)
- DRAM control signal: XRAS/XCAS/XOE/XWE terminals (Pins 122 to 125)

Audio data output to STR circuit (When H.A.T.S. is ON)
- Audio data: DATA terminal (Pin 22)
- Signal clock: 512FSI terminal (Pin 2), BCKO terminal (Pin 20), LRCKO terminal (Pin 21)

(6) PLL circuit (LINK)

The MDS-LSA1 and STR-LSA1 receives, records or plays sounds from other devices. Consequently, the clocks must be generated according to the sampling frequency (fs) of the audio signals received. The signal is therefore synchronized by the PLL circuit mounted externally to LINK.

SYTO terminal (Pin 26) ..... When the i.LINK signal is received, the 1/8 fs clock of the signal received is output.
When fs is 44.1 kHz: 5.51 kHz.

PLLCKI terminal (Pin 27) ..... The 256 fs clock generated in the external PLL circuit is input.
When fs is 44.1 kHz: 11.289 MHz.

1/8OUT terminal (Pin 25) ..... The 1/2048 signal of the signal input to the PLLCKI terminal (Pin 27) is output.
When fs is 44.1 kHz: 5.51 kHz.

(Repair Tips) When i.LINK audio signal cannot be received

When i.LINK audio signal cannot be received, check the SYTO terminal of LINK (Pin 26). If the presence of a clock which is 1/8 times the sampling frequency can be confirmed at the SYTO terminal, it means that the i.LINK circuit is performing reception operations normally, and the error is due to malfunction of the digital audio processing circuit after the i.LINK circuit. If the clock cannot be confirmed at the SYTO terminal, check the signal path between PHY and LINK and the PLL circuit.

MEMO

SONY

9-929-531-31

Sony Corporation
Audio Entertainment Group

2001C0900-1
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