MN66279RSC

1. Type

Signal processing LSI for CDs (Compact Discs)

2. Overview

MN662790RSC is a signal processing LSI for CDs which is applicable to 4x-speed playback. It incorporates optical servo (focus, tracking and traverse servos) processing function, digital signal processing function (EFM demodulation and error correction), digital servo processing function for spindle motor, a digital filter and D/A converter. All the processing functions after the head amplifier (RF amplifier) are incorporated into a single chip. In addition, it incorporates clock generation and error correction circuits to increase the playability and is applicable to video CD playback.

3. Functions and features

(Optical servo)

- Focus (Fo), tracking (Tr) and traverse (TRV) servos
  (f_S: Fo=44.1 kHz, Tr=44.1 kHz)
- Automatic adjustment functions (Fo/Tr gain, Fo/Tr offset, Fo/Tr balance)
- On-chip D/A converter for drive voltage output
- Provided with a countermeasure for dropout
- Provided with anti-shock function
- Provided with track cross detecting function
- On-chip track cross counter

(Digital signal processing)

- Containing DSL and PLL
- Provided with a frame synchronous detection/protection/interpolation
- Subcode data processing
  Q-data CRC check
  On-chip Q-data register
- CD-TEXT interface function
  On-chip CD-TEXT register (144 bits × 2)
- CIRC error correction
  C1 decoder : double error correction
  C2 decoder : triple error correction, quadruple error correction
  On-chip de-interleaving 16K RAM
- Audio data interpolation processing
  4-sampling average value interpolation and previous value hold
- Digital attenuation (256 levels)
- Soft attenuation (256 levels)
- Soft muting
- Digital audio interface (EIAJ format)
- Audio data serial interface (Input/Output)
- Microcomputer serial interface
- General-purpose I/O port (4 pins)
- Audio data peak level detection function

(Spindle motor servo)
- CLV digital servo
- Servo gain setting function

(Audio Circuit)
- 8x-oversampling digital filter
- On-chip D/A converter (1-bit DAC)
- On-chip differential OP amp (2nd-order low-pass filter)

(Others)
- 4x-speed playback
- Disc rotation synchronizing playback (jitter-free) function (4x-speed±50 %)
- Oscillation stop mode
- Power management mode
- Playback pitch control function

4. Package

80-pin quad flat package (LQFP080-P-1414A)

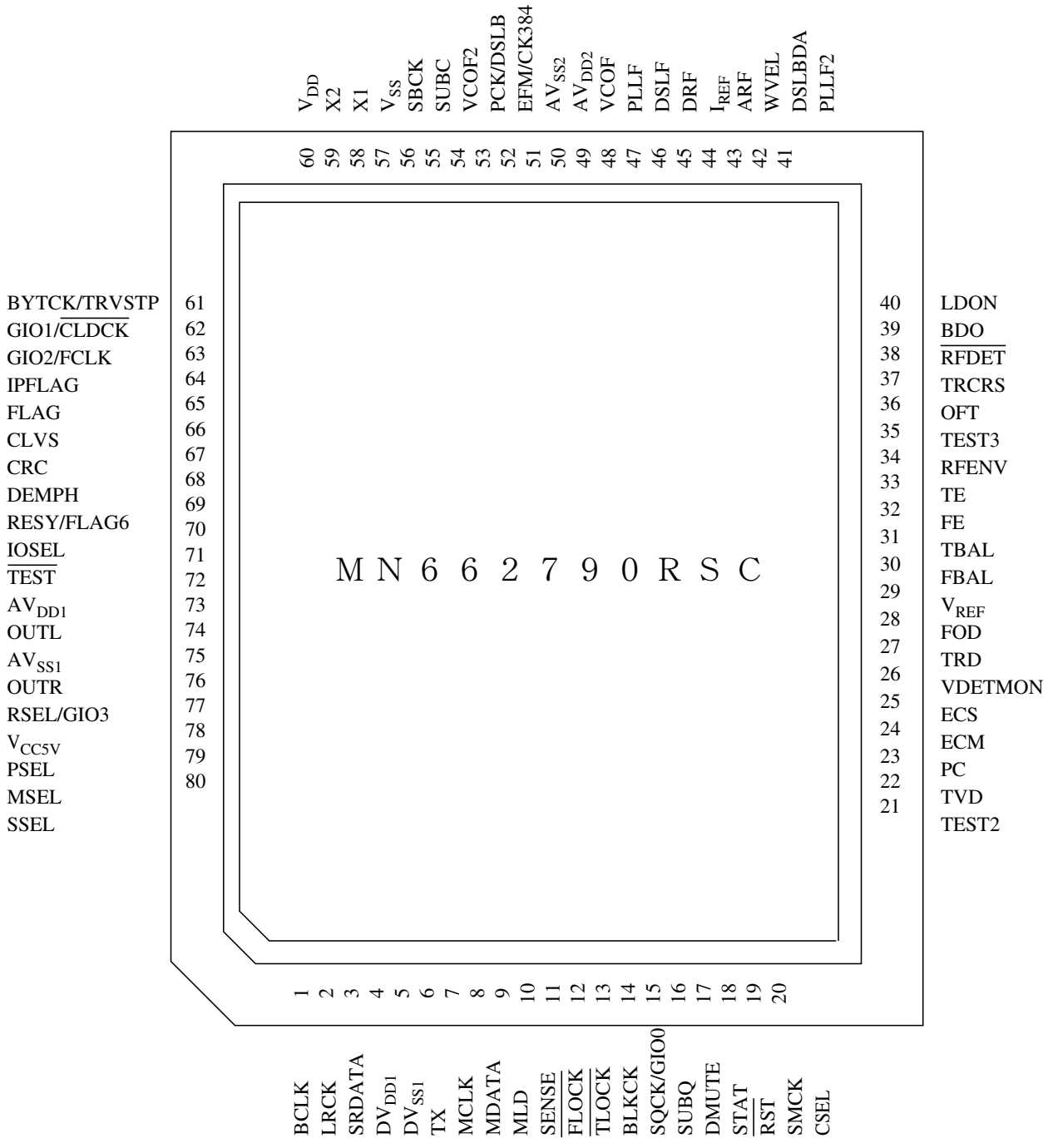
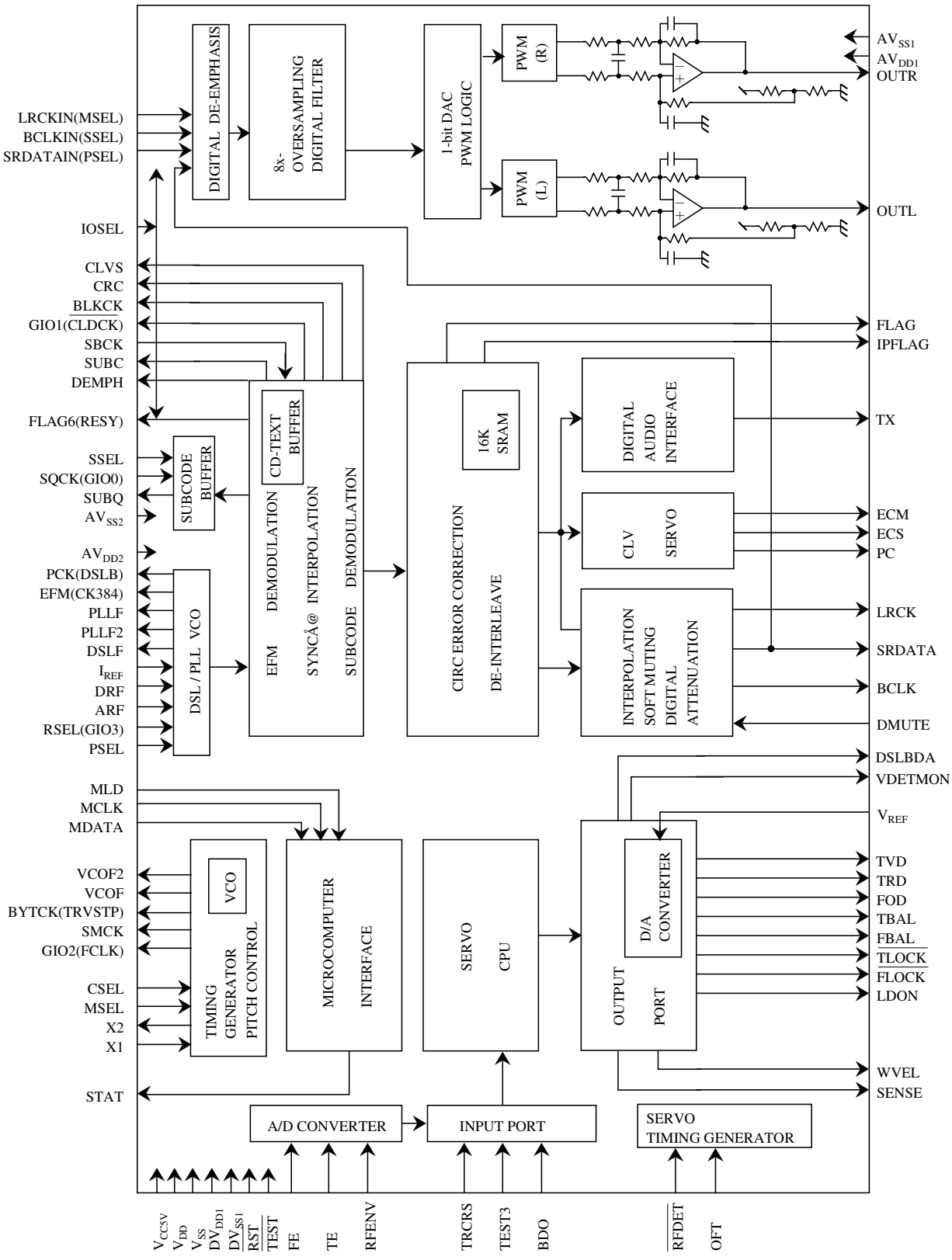


Figure 1 Pin Assignment

5. Block diagram



6. Pin descriptions

No.	Symbol	I/O	Pin for 5-V input	Function
1	BCLK	O		Bit clock output for SRDATA
2	LRCK	O		L/R identification signal output
3	SRDATA	O		Serial data output
4	DV_{DD1}	I		Power supply for digital circuits
5	DV_{SS1}	I		Ground for digital circuits
6	TX	O		Digital audio interface output signal
7	MCLK	I	○	Microcomputer command clock signal input (Latches the data at a rising edge)
8	MDATA	I	○	Microcomputer command data signal input
9	MLD	I	○	Microcomputer command load signal input L: Load
10	SENSE	O		Sense signal output (OFT, FESL, $\overline{\text{ACEND}}$, $\overline{\text{AJEND}}$, SFG)
11	$\overline{\text{FLOCK}}$	O		Focus servo pull-in signal (L: Pull-in status)
12	$\overline{\text{TLOCK}}$	O		Tracking servo pull-in signal (L: Pull-in status)
13	BLKCK	O		Subcode block clock signal (f_{BLKCK} = 75 Hz) At command execution: CD-TEXT data reading enable signal (DQSY) output
14	SQCK/ GIO0	I	○	At default value: External clock input for subcode Q register At command execution: General-purpose I/O port In CD-TEXT 2 mode: Clock input for TEXT data reading
15	SUBQ	O		Subcode Q-data output In CD-TEXT 2 mode: TEXT data output
16	DMUTE	I	○	Muting input H: Mute
17	STAT	O		Status signal (CRC, STCNT, CLVS, TTSTOP, JCLVS, SQOK, FLAG6, SENSE, $\overline{\text{FLOCK}}$, $\overline{\text{TLOCK}}$, rotating speed data, FCLV, SUBQ, SYFLG) In CD-TEXT 3 mode: Subcode Q and TEXT data output
18	$\overline{\text{RST}}$	I	○	Reset input L: Reset
19	SMCK	O		8.4672-MHz clock signal output at MSEL = H 4.2336-MHz clock signal output at MSEL = L
20	CSEL	I	○	Oscillation frequency selection pin H: 33.8688 MHz L: 16.9344 MHz

No.	Symbol	I/O	Pin for 5-V input	Function
21	TEST2	O		TEST pin 2 Normal: OPEN
22	TVD	O		Traverse drive output
23	PC	O		Spindle motor ON signal output L: ON (default)
24	ECM	O		Spindle motor drive signal (Forced mode output) 3-state output
25	ECS	O		Spindle motor drive signal (Servo error signal output)
26	VDETMON	O		Vibration detection monitor output
27	TRD	O		Tracking drive output
28	FOD	O		Focus drive output
29	V_{REF}	I		Reference voltage for D/A output stage (TVD, ECS, TRD, FOD, FBAL, TBAL, TOFS)
30	FBAL	O		Focus balance adjustment output
31	TBAL	O		Tracking balance adjustment output
32	FE	I		Focus error signal input (Analog input)
33	TE	I		Tracking error signal input (Analog input)
34	RFENV	I		RF envelope signal input (Analog input)
35	TEST3	I		TEST pin 3 Normal: Fixed to "L"
36	OFT	I		Off track signal input H: Off track
37	TRCRS	I		Track cross signal input (Analog input)
38	$\overline{\text{RFDET}}$	I		RF detection signal input L: Detection
39	BDO	I		Dropout signal input H: Dropout
40	LDON	O		Laser ON signal output H: ON
41	PLLF2	I/O		Selector pin for PLL loop filter characteristics
42	DSLBDA	O		DSL balance output (D/A output)
43	WVEL	O		2x-speed status signal output L: 2x-speed
44	ARF	I		RF signal input

No.	Symbol	I/O	Pin for 5-V input	Function
45	I_{REF}	I		Reference current input pin
46	DRF	I		Bias pin for DSL
47	DSLF	I/O		DSL loop filter pin
48	PLLF	I/O		PLL loop filter pin
49	VCOF	I/O		VCO loop filter pin
50	AV_{DD2}	I		Power supply for analog circuits (For DSL, PLL, D/A output stage and A/D)
51	AV_{SS2}	I		Ground for analog circuits (For DSL, PLL, D/A output stage and A/D)
52	EFM/ CK384	O		At IOSEL = H: EFM signal output At IOSEL = L: 16.9344-MHz clock output for crystal oscillation $384f_S$ output for signal processing (VCO clock output in jitter-free operation) (Select crystal oscillation or signal processing with command setting)
53	PCK/ DSLB	O		PLL extraction clock output or DSL balance output (PWM output) (f_{PCK}=4.3218 MHz)
54	VCOF2	I/O		VCO loop filter pin for the digital servo clock generation at 33.8688 MHz The external circuit is required for crystal oscillation at 16.9344 MHz.
55	SUBC	O		Subcode serial output In CD-TEXT 1 mode: TEXT data output
56	SBCK	I	○	Clock input for subcode serial output In CD-TEXT 1 mode: Clock input for TEXT data reading
57	V_{SS}	I		Ground for oscillation circuit
58	X1	I		Crystal oscillation circuit input pin (f=16.9344 MHz, 33.8688 MHz)
59	X2	O		Crystal oscillation circuit output pin (f=16.9344 MHz, 33.8688 MHz)
60	V_{DD}	I		Power supply for oscillation circuit
61	BYTCK/ TRVSTP	O		At IOSEL = H: Byte clock signal output At IOSEL = L: Traverse stop signal output H: STOP mode
62	GIO1/ $\overline{\text{CLDCK}}$	O		At default value: General-purpose I/O port At command execution: Subcode frame clock signal output (f_{CLDCK}=7.35 kHz)
63	GIO2/ FCLK	O		At default value: General-purpose I/O port At command execution: Crystal frame clock signal output (f_{FCLK}=7.35 kHz)
64	IPFLAG	O		Interpolation flag signal output H: Interpolation
65	FLAG	O		Flag signal output

No.	Symbol	I/O	Pin for 5-V input	Function
66	CLVS	O		Spindle servo phase synchronous status signal output H: CLV L: Rough servo
67	CRC	O		At default value: Subcode CRC check result output H: OK L: NG
68	DEMPH	O		De-emphasis detecting signal output H: ON
69	RESY/ FLAG6	O		At IOSEL = H: Frame re-sync signal RESY output H: Synchronous L: Asynchronous At IOSEL = L: RAM address reset signal FLAG6 output for error correction and de-interleave L: Address reset generated
70	IOSEL	I		Mode selector pin
71	$\overline{TEST}$	I		Test pin (Normal: H)
72	AV_{DD1}	I		Power supply for analog circuits (For audio output stage) (Commonly used for L-ch and R-ch)
73	OUTL	O		L-ch audio output
74	AV_{SS1}	I		Ground for analog circuits (For audio output stage) (Commonly used for L-ch and R-ch)
75	OUTR	O		R-ch audio output
76	RSEL/ GIO3	I	○	At default value: RF signal polarity specification pin When the bright level is "H", RSEL=H. When the bright level is "L", RSEL=L. At command execution: General-purpose I/O port RF signal polarity is specified with command setting. In CD-TEXT 1 or 2 mode: TEXT data reading enable signal (DQSY) output
77	V_{CC5V}	I	○	5-V power supply applied to pins for 5-V input
78	PSEL	I	○	At IOSEL = H: Test pin (Normal: L) At IOSEL = L: SRDATA input
79	MSEL	I	○	At IOSEL = H: SMCK pin output frequency selector pin H: SMCK = 8.4672 MHz L: SMCK = 4.2336 MHz At IOSEL= L: LRCK input H: L-ch data, L: R-ch data SMCK = Fixed at 4.2336 MHz
80	SSEL	I	○	At IOSEL = H: SUBQ pin output mode selector pin H: Q-code buffer working mode L: $\overline{CLDCK}$ synchronous mode At IOSEL = L: BCLK input Q-code buffer working mode fixed

7. Function description (Table of contents)

7-0. Contents of functions amended from MN662748

7-0 (1) Digital servo section

1) Initialization
◎ Initialization with SYS command after the standby time (0.1 s) preset by the on-chip timer has elapsed

2) Automatic adjustment
- Abolishment of Tr offset external feedback adjustment
- Fo/Tr offset adjustments batch processing only
- Setting of the convergence gain for Fo balance adjustment (1/8, 1/4, 1/32, 1/16)
- Abolishment of Tr rough gain adjustment with TROFF
- Selection of the convergence conditions for Tr balance adjustment

◎ Hunting preventive function in Fo balance adjustment

3) Servo
◎ Servo sampling frequency: 44.1 kHz
◎ Vibration detection with software
- TRV dead-zone amplifier mode selectable
- Unified Tr servo output (TRD and KICK)
- Unified TRV servo output (TVD and TRV)
- TVD output gain selectable
- Fo servo filter Z^{-N} setting (N: Fixed to 2)
- Selecting Fo servo dropout processing (0 mute only)
- Selecting Fo disc detecting frequency (5.4 Hz, 2.6 Hz)
- Tr servo output stage noise shaver ON/OFF (Fixed to ON)
- Selecting Tr servo dropout processing (0 mute only)
- Selecting TRV loop filter (Type A only)
- Smoothing TRV servo output
- OFT input noise filter turned ON/OFF with a command

◎ Setting of high-speed Fo pull-in operation when turning Fo ON from OFF state
◎ Setting of dropout processing during KICK operation
◎ Trigger function at vibration detection
- Abolishment of Fo servo's perfect integral and limited characteristics selection (Perfect integral characteristic only)
- Abolishment of Tr servo's perfect integral and limited characteristics selection (Perfect integral characteristic only)
- Change of servo parameter exponent part format (FEXP, TEXP)

4) Access
- TCNT (track count move) processing with software
- Outputting TRD during TCNT (track count move) (0 only)

5) DTMS, DTSM
- Possible to set Tr gain constant limiter arbitrarily for initial Tr gain constant and Tr fine gain adjustments
- Possible to set Fo gain constant limiter arbitrarily for initial Fo gain constant and Fo fine gain adjustments

◎ Possible to set band-pass filter constants and a detecting level for vibration detection

7-0 (2) Signal processing section

1) Signal processing over the system

Applicable for VIDEO CDs

◎ Error correction method
- Selectable between double (C1) and triple (C2) corrections, and double (C1) and quadruple (C2) corrections
- C1 flag discrimination condition at C2 correction selectable

◎ PLL circuit for VIDEO CDs (Digital PLL)

Other functions

◎ Audio interpolation processing 4-sampling interpolation
◎ Addition of CD-TEXT output format 4 mode
◎ Peak data output function (Same as the specification for MN662780)
◎ Audio output level attenuation function
◎ Pitch control function (±50 % of 1x-, 2x- and 4x-speed)
◎ Error flag counting function (selectable between FLAG0 and IPFLAG)
◎ TX output generation from audio DAC external input data (Conventional method is also selectable)

2) DSL, PLL

◎ PLLF current selection mode (×1, ×0.75, ×0.5, ×1.25)
◎ PLL frequency dividing function
◎ Digital PLL control
◎ Charge pump current adjusting function

3) Digital audio interface (TX)

◎ Bit V control of TX output
◎ Generation of TX output from DF input data

4) Spindle servo

◎ CLV synchronization establishment detecting flag

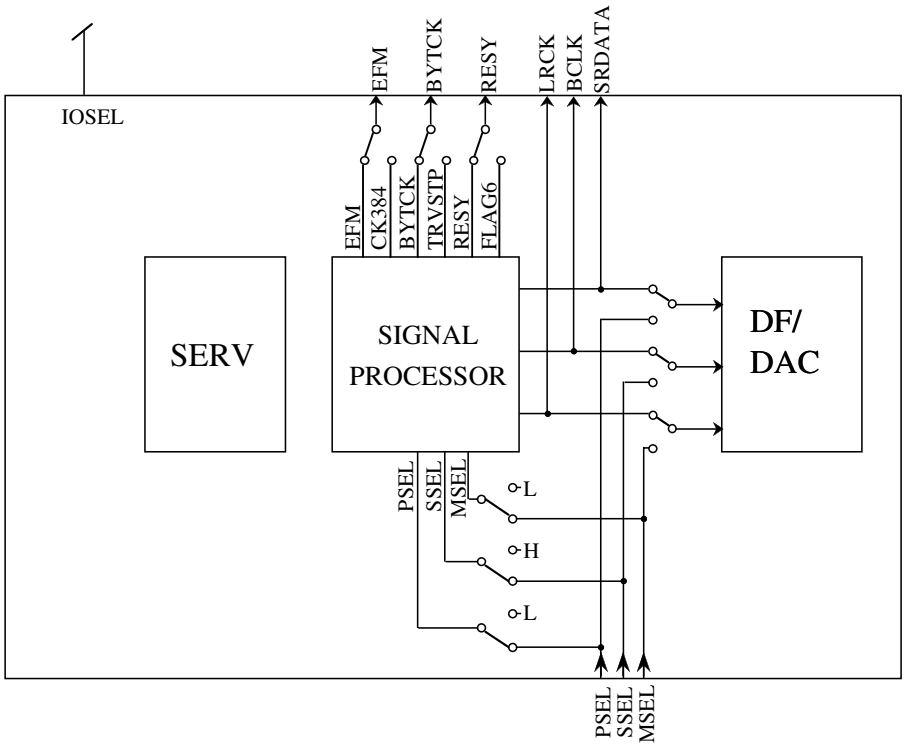
7-0 (3) Digital filter (DF) and D/A converter (DAC) sections

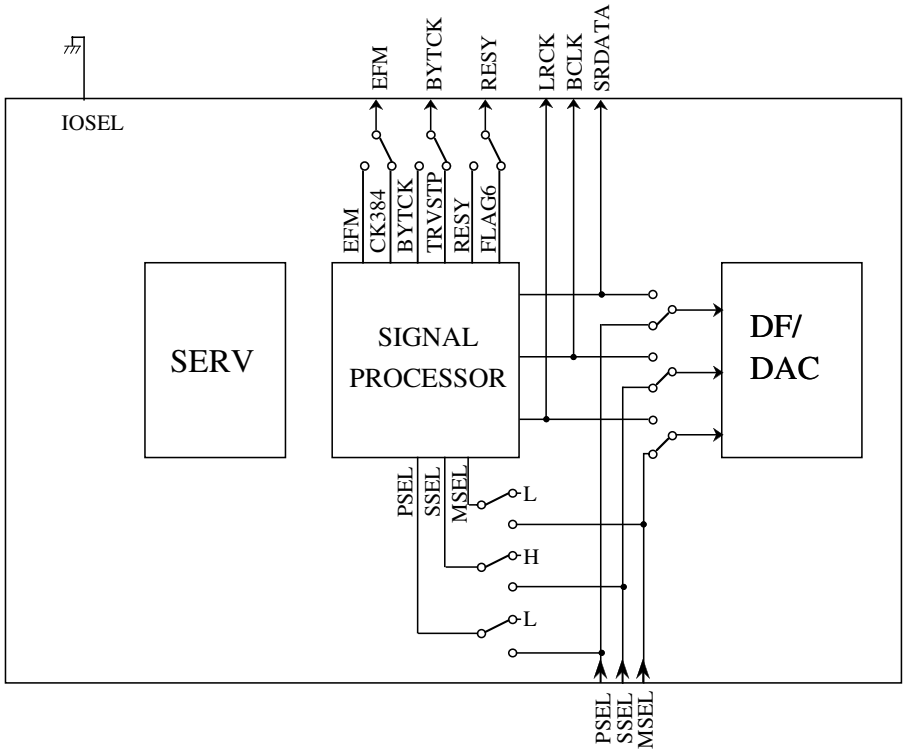
◎ Newly added digital filter calculation constants
- 1-bit D/A converter

7-0 (4) The whole system

◎ PMCK and PLAY pins eliminated
◎ V_{CC5V} pin for 5-V input added
◎ 3.3-V operation of internal circuit
◎ Digital input pins for 5-V input

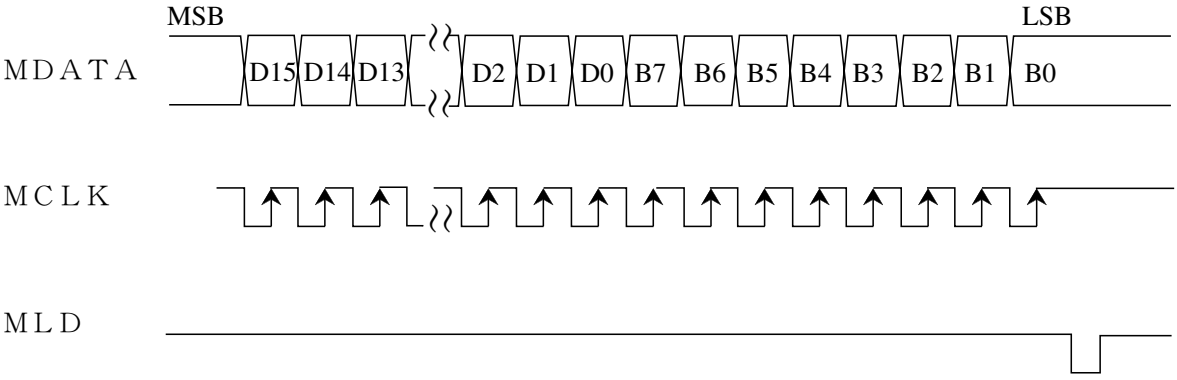
Setting the LSI Operation Mode by the IOSEL Pin





7-1. Microcomputer interface

Each mode can be set by inputting the 16-bit data (D15 to 0) and 8-bit command (B7 to 0) starting from the MSB in 3 inputs of MDATA, MCLK and MLD at the timing as shown in Figure 7-1-1.



Note) ・ Data is determined at the "L" level of MLD.
・ MDATA, MCLK and MLD are invalid while $\overline{RST}$ is "L".
・ All commands are initialized by setting $\overline{RST}$ to "L".
・ While MLD is set to "L", MCLK will be canceled if it rises.

(Timing)

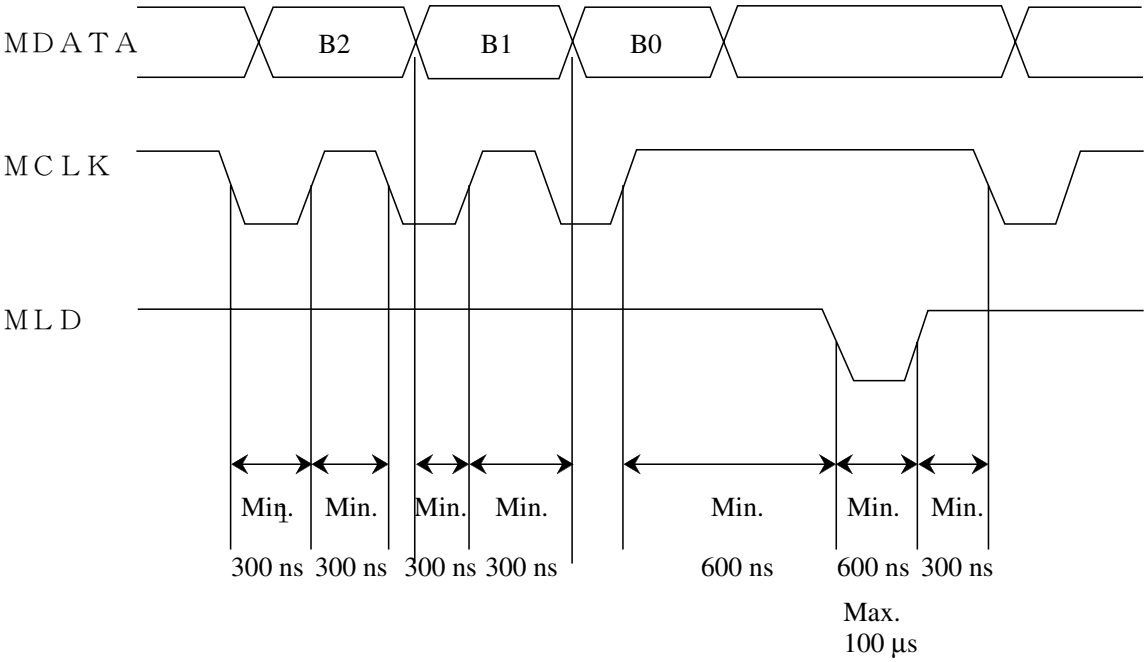


Figure 7-1-1

7-1 (1) List of microcomputer commands

(1-1) Servo processor

Table 7-1-1 (1)

Control Target	MDATA B7	B6	B5	B4	B3	B2	B1	B0	Symbol	Function	SENSE output	Data	At reset	Chapter
Initiali-zation	1	1	1	1	0	1	0	1	SYS	System setting	SFG	16 bits		
					0	1	1	0		RESERVED				
Automatic adjust-ment	1	1	1	1	0	1	1	1	ABC1	Fo balance adjustment	$\overline{\text{AJEND}}$	—		
					1	0	0	0	ADA	Stopping automatic adjustment	$\overline{\text{AJEND}}$	—		
					1	0	0	1	AOC	Offset adjustment (Fo, Tr)	$\overline{\text{AJEND}}$	—		
					1	0	1	0		RESERVED		—		
					1	0	1	1	ABC2	Tr balance adjustment	$\overline{\text{AJEND}}$	—		
					1	1	0	0	AGC1	Fo rough gain adjustment	$\overline{\text{AJEND}}$	—		
					1	1	0	1	AGC2	Tr rough gain adjustment	$\overline{\text{AJEND}}$	—		
					1	1	1	0	FAGC	Fo fine gain adjustment	$\overline{\text{AJEND}}$	—		
					1	1	1	1	TAGC	Tr fine gain adjustment	$\overline{\text{AJEND}}$	—		
Data setting	1	1	1	1	0	0	1	0	DTMS	Data write	$\overline{\text{WTEND}}$	16 bits		
					0	1	0	0	DTSM	Data read	DATA	8 bits		
Optical servo	1	1	1	0	0	0	0	0	STB	Standby	OFT	—	○	
					0	0	0	1		RESERVED				
					0	0	1	0	DDT	Disc detection	FESL	—		
					0	0	1	1	TOF	Fo ON, Tr OFF	FESL	—		
					0	1	0	0	PLY	Fo ON, Tr ON	OFT			
					0	1	0	1	PLY2	Fo ON, Tr ON (TRVSTP disabled)	OFT			
TRV servo	1	1	1	0	1	0	0	0	TVS	TRV stop		—	○	
					1	0	0	1		RESERVED				
					1	0	1	0	TVF	TRV forward feed	No change	—		
					1	0	1	1	TVR	TRV reverse feed		—		
					1	1	0	0	TVP	TRV play				
Access	1	1	1	1	0	0	0	0	ACA	Stopping access operation	$\overline{\text{ACEND}}$			
					0	0	0	1	KICK	Kick	$\overline{\text{ACEND}}$	16 bits		
					0	0	1	1	TCNT	Track count move	$\overline{\text{ACEND}}$	16 bits		

(1-2) Signal processing

Table 7-1-1 (2)

Control Target	MDATA B7	B6	B5	B4	B3	B2	B1	B0	Symbol	Function	Data	At reset	Chapter
Spindle	0	0	0	1	1	×	×	×		RESERVED			
					0	×	×	×		RESERVED			
					×	1	×	×	TTON	Turntable ON (H)	—		
					×	0	×	×	TTOFF	Turntable OFF (L)	—	○	
					×	×	0	0	STOP	Free-running	—	○	
					×	×	0	1	ACC	Acceleration	—		
					×	×	1	0	BRAKE	Deceleration	—		
					×	×	1	1	PLAY	Normal play	—		
TX output Audio output	0	0	1	0	1	×	×	×		Digital I/F Bit C (28) SET	—		
					0	×	×	×		Digital I/F Bit C (28) RESET	—	○	
					×	1	×	×		Digital I/F Bit C (29) SET	—		
					×	0	×	×		Digital I/F Bit C (29) RESET	—	○	
					×	×	0	0		Normal output (0dB)	—		
					×	×	0	1		Soft muting	—		
					×	×	1	0		Digital attenuation	—		
					×	×	1	1		Soft attenuation			
Audio output	0	0	1	1	×	0	×	×	NOS	WVEL=L Normal-speed playback	—	○	
					×	1	×	×	DOS	WVEL=H 2x-speed playback	—		
					×	×	0	×		LRCK signal (R-ch=L, L-ch=H)	—	○	
					×	×	1	×		LRCK signal (R-ch=H, L-ch=L)	—		
					0	×	×	0		Audio mode (Ⅰ)	—	○	
					0	×	×	1		Audio mode (Ⅱ)	—		
					1	×	×	0		CD-ROM mode	—		
TX output	0	1	0	0	0	×	0	0		TX pin output enabled	—	○	
					1	×	0	0		TX pin output disabled ("L" is fixed)	—		
					×	0	0	0		Digital I/F category code = CD mode	—	○	
					×	1	0	0		Digital I/F category code = general mode	—		
	0	1	0	0	0	0	0	1		Audio output control (I)	16 bits		
					0	0	1	0		Digital/Audio I/F control	16 bits		
					0	0	1	1		General-purpose I/O port control	16 bits		
					0	1	0	1		Spindle control	16 bits		
					0	1	1	0		Audio output control (II)	16 bits		
					0	1	1	1		Audio output control (III)	16 bits		
					1	0	0	1		CLV speed setting	16 bits		
					1	0	1	0		RESERVED	16 bits		
					1	0	1	1		DSL and PLL controls (I)	16 bits		
					1	1	0	1		DSL and PLL controls (II)	16 bits		
					1	1	1	0		Digital PLL control	16 bits		

Table 7-1-1 (3)

Control Target	MDATA B7	B6	B5	B4	B3	B2	B1	B0	Symbol	Function	Data	At reset	Chapter
SRDATA Audio output	0	1	0	1	AL3 to 0					Attenuation level (lower 4 bits)		0 0 0 0	
	0	1	1	0	AL7 to 4					Attenuation level (upper 4 bits)		0 1 0 0	
STAT pin output	0	1	1	1	0	0	0	0		STAT output CRC		○	
					0	0	0	1		STAT output STCNT			
					0	0	1	0		STAT output CLVS			
					0	0	1	1		STAT output TTSTOP (during TTOFF)			
					0	0	1	1		STAT output JCLVS (during TTON)			
					0	1	0	0		STAT output SQOK			
					0	1	0	1		STAT output switching	3 bits		
					0	1	1	0		STAT output disc rotating speed	16 bits		
					0	1	1	1		STAT output FCLV			
					1	0	0	0		STAT output SUBQ			
					1	0	0	1		STAT output SYFLG			
					1	0	1	0		STAT output EDATA			

・SENSE signal

SENSE signal can be monitored through STAT pin. The meaning of SENSE signal varies with the input command. The meanings are described below.

OFT	Off-track input signal is output as it is.
FESL	It is set to "H" when the absolute value of the focus error signal amplitude exceeds 30 [LSB] by executing the disc detecting command.
$\overline{\text{ACEND}}$	It is set to "L" when the access terminates and the pull-in operation of the tracking servo starts.
$\overline{\text{AJEND}}$	It is set to "L" when automatic adjustment terminates.
$\overline{\text{WTEND}}$	It is set to "L" when data write terminates normally.
DATA	The contents of the RAM of the specified address is output beginning with MSB by inputting MCLK a minimum of 50 ms after MLD is set to "L" with the data read command, DTSM, sent out for data reading. Refer to Figure 7-1-4.

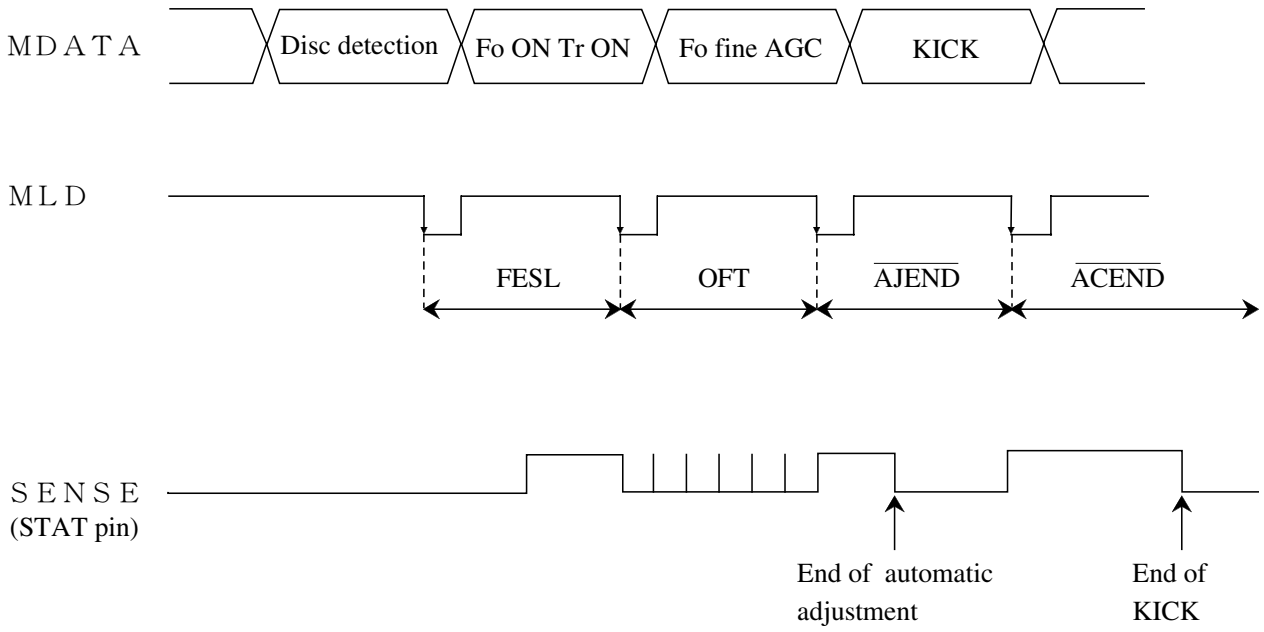


Figure 7-1-2 Switching of SENSE output

7-1 (2) Initialization

After clearing $\overline{RST}$, the system waits for a data write command (DTMS) and SYS command.

1) After clearing $\overline{RST}$, execute the data write command first.
The data write command is composed of the following three bytes, which is different from the regular format (see page 22).

D15	D14	D13	D12	D11	D10	D9	D8	SET0＝×××× ×××1 (B)
D7	D6	D5	D4	D3	D2	D1	D0	VSET＝×××× ×××× (B)
B7	B6	B5	B4	B3	B2	B1	B0	DTMS＝1111 0010 (B)

That is, SET0 (various system settings) data is stored in the upper 8 bits of the 16-bit data, and VSET (anti-vibration mode selection) data is stored in the lower 8 bits.

2) After the data write command (DTMS) is processed, the SENSE signal ($\overline{WTEND}$) is set to "L" and it is in the standby status for the SYS command.

Unlike conventional models, no system settings are possible with the SYS command. This is due to the expansion of the DTMS/DTSM functions. Execute the following command, however, after checking that the SENSE signal is set to "L". This is for the protocol assurance of the SENSE signal with the mechanical controller.

When the SYS command MDATA 1111 0101 is accepted, the SENSE signal is set to "H" and processing of the SYS command starts. When the processing completes, the SENSE signal is set to "L" to enter the normal operation loop.

Table 7-1-2 indicates the default values of system setting. The default value of each item is changeable with the DTMS command.

Note)
If the data write command (DTMS) is not executed within 743 ms after starting the standby status for the data write command (DTMS) and the SYS command, the system setting is performed with the default value and enters the normal operation loop.

Be aware that initial SET0 data and VSET data are written in a special format that is entirely different from the format used for writing usual data. In initial setting, SET0 and VSET are set at the same time only by sending a 3-byte command once, while in normal write, SET0 and VSET are set separately using a 3-byte command.

Timing chart is shown in Figure 7-1-3.

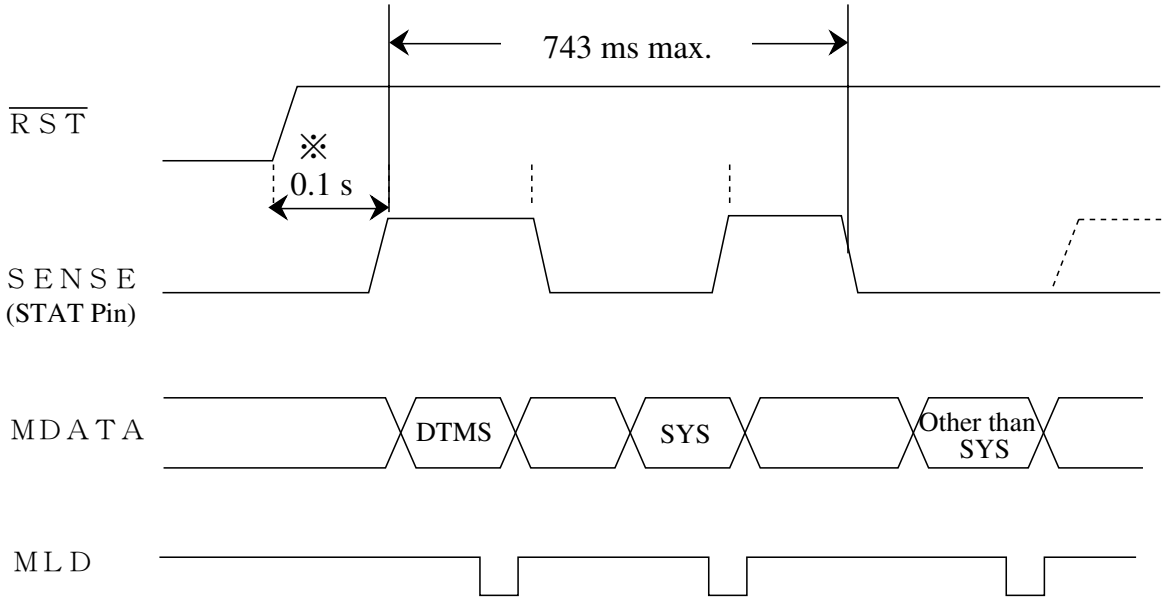


Figure 7-1-3 Timing chart in initial setting

※ A 0.1-s standby time is not necessary to send the DTMS command and the SYS command after reset clearance. To ensure system stability after turning on the power, send the DTMS command and the SYS command after SENSE is set to "H".

Table 7-1-2

Item	Default value
Gain for tracking variable gain amp	+6 [dB]
Gain for focus variable gain amp	+12 [dB]
Output amplitude for focus search	±22 [LSB]
Fail-safe value for tracking servo	±72 [LSB]
Standby time after track count move	50 [ms]
Traverse drive constant	2
Traverse drive dead-zone	±24 [LSB]
Optical servo	Standby
Traverse servo	Stop
2x-speed mode	NOS
Spindle servo	Turntable OFF
	STOP (Free-running)
TX pin output	Enabled
STAT pin output	CRC output

Note) To obtain the waveform shown in the above timing chart, the MLD pulse width should be 10 µs or less. If it is more than the value, SENSE clear ("H" → "L") by the SYS command in the above timing may not be performed.

7-1 (3) Data setting for servos

[1] Data write (DTMS)

Various features can be achieved by writing various characteristics of the optical servo system from an external microcomputer to this LSI.

DTMS command is used to write the data such as servo parameters.

(Applications)

(A) Setting of automatic adjustment value
(B) Setting of the optical servo loop characteristics including the characteristics for anti-vibration
(C) Setting of gain crossover for the optical servo loop
(D) Mode selection for anti-vibration
(E) Various system settings
(F) Various settings for optical servo system

(MDATA format)

D7	D6	D5	D4	D3	D2	D1	D0	: Data
A7	A6	A5	A4	A3	A2	A1	A0	: Address (Label specified)
1	1	1	1	0	0	1	0	: Command (DTMS)

Note)

- Use the DTMS command in the STANDBY or PLAY mode.
- If you write data successively, wait at least 50 µs after each data writing so that the microcomputer finishes DSP processing and becomes ready for writing next data.

[2] Data read (DTSM)

・This LSI can read out the parameters such as automatic adjustment results of the optical servo with the DTSM command.

(MDATA format)

A7	A6	A5	A4	A3	A2	A1	A0

: Address (Label specified)

1	1	1	1	0	1	0	0

: Command (DTSM)

(Data output format)

Input an address and a command, and after a lapse of 50 µs or more since setting MLD=L, input MCLK, thus enabling to read data from STAT pin. (SENSE output)

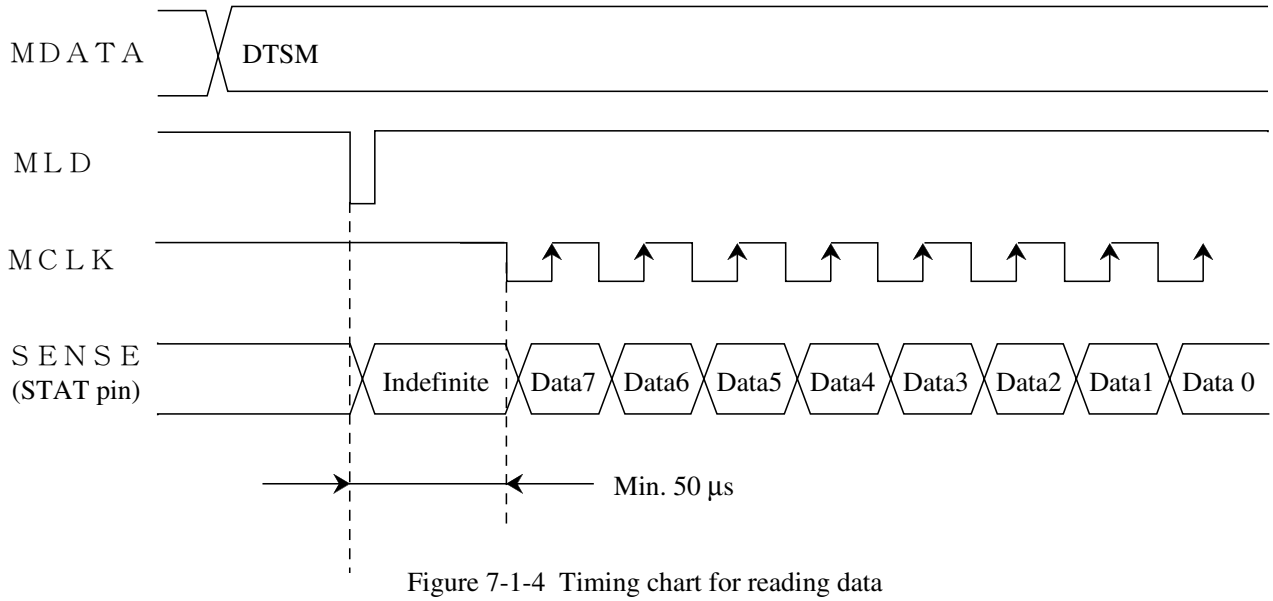


Figure 7-1-4 Timing chart for reading data

Note) Perform either in the STANDBY or PLAY mode.

(List of DTMS addresses)

Table 7-1-3 (1)

Address (HEX) (A7 to A0)	Label	Application	Reference page
0 0	F G 0	Focus gain automatic adjustment value in normal-speed mode (for setting use)	25
0 1	F E X P 0	Focus gain automatic adjustment value in normal-speed mode (for setting use)	25
0 2	F B A L	Focus balance automatic adjustment value	25
0 3	F O F S	Focus offset automatic adjustment value	25
0 4	T G 0	Tracking gain automatic adjustment value in normal-speed mode (for setting use)	25
0 5	T E X P 0	Tracking gain automatic adjustment value in normal-speed mode (for setting use)	25
0 6	T B A L	Tracking balance automatic adjustment value	25
0 7	T O F S	Tracking offset automatic adjustment value	25
0 8	F C	Focus phase compensation constant	26
0 9	F R	Focus low-band compensation constant	26
0 A	T C	Tracking phase compensation constant	26
0 B	T R	Tracking low-band compensation constant	26
0 C	F C 2	Focus phase compensation constant at vibration	26
0 D	F R 2	Focus low-band compensation constant at vibration	26
0 E	T C 2	Tracking phase compensation constant at vibration	26
0 F	T R 2	Tracking low-band compensation constant at vibration	26
1 0	G S E T	Gain crossover setting	28
1 1	V S E T	Mode selection for anti-vibration	29
1 2	S E T 0	Various system settings	31
1 3	S E T 1	Various system settings	32
1 4	S E T 2	Various system settings	33
1 5	S E T 5	Various system settings	35
1 6	F E S	Focus gain disturbance amplitude	25
1 7	T E S	Tracking gain disturbance amplitude	25
1 8	C R A M 2	Focus search amplitude	38
1 9	S D	Search direction	38
1 A	K S	Kick speed / Kick brake timing	39
1 B	T V G	Traverse gain constant in tracking brake operation	40
1 C	C R A M 3	Fail-safe value for tracking servo	38
1 D	C R A M 4	Tracking balance disturbance adjustment value	38
1 E	S E T 3	Various system settings	34
1 F	D E D 0	Traverse drive dead-zone	40

Table 7-1-3 (2)

Address (HEX) (A7 to A0)	Label	Application	Reference page
2D	FG2	Focus gain constant mantissa part at vibration (for setting use)	30
2E	FEXP2	Focus gain constant exponent part at vibration (for setting use)	30
35	TG2	Tracking gain constant mantissa part at vibration (for setting use)	30
36	TEXP2	Tracking gain constant exponent part at vibration (for setting use)	30
39	GLF1	Focus gain constant upper limit mantissa part	43
3A	GLF2	Focus gain constant upper limit exponent part	43
3B	GLF3	Focus gain constant lower limit mantissa part	43
3C	GLF4	Focus gain constant lower limit exponent part	43
3D	GLT1	Tracking gain constant upper limit mantissa part	43
3E	GLT2	Tracking gain constant upper limit exponent part	43
3F	GLT3	Tracking gain constant lower limit mantissa part	43
40	GLT4	Tracking gain constant lower limit exponent part	43
49	SETKC	Track count and KICK noise elimination width	40
4A	SETTB	Various system settings	36
4B	KCCNT	Inverted pulse width with tracking brake and servo control turned on	41
		Initial accelerating time with tracking brake turned on	41
61	PDK	Convergence gain setting in fine gain adjustment	42
78	KICK	KICK output level in normal operation	41
79	TRV	Traverse output level	41
7A	KICK2	KICK output level when servo is pulled in	41
7B	VSLT	Vibration detecting level mantissa part	42
7C	PHSU	Number of disturbance waves setting in fine gain adjustment	42
80	—	Focus and tracking gains setting for normal gain	37
81	—	Focus and tracking gains setting for forced gain-up	37
AA	—	Software reset	37

※ Do not write illegal data in any of the above addresses, otherwise the existing data in the address is overwritten and the operation of this LSI is not guaranteed.

(A) Setting of automatic adjustment value

FG0	(Focus gain mantissa part)	,	TG0	(Tracking gain mantissa part)
FEXP0	(Focus gain exponent part)	,	TEXP0	(Tracking gain exponent part)
FBAL	(Focus balance adjustment value)	,	TBAL	(Tracking balance adjustment value)
FOFS	(Focus offset adjustment value)	,	TOFS	(Tracking offset adjustment value)
FES	(Disturbance amplitude in focus gain adjustment)			
TES	(Disturbance amplitude in tracking gain adjustment)			

Table 7-1-3 (3)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	00	F2	Focus gain constant (FG0) (8-bit mantissa) (1 to 255)	128
D7 D6 D5 D4 D3 D2 D1 D0	01		Focus gain constant (FEXP0) (8-bit exponent) (16, 32, 64 and 128 only) (Focus gain constant = mantissa / exponent)	32
D7 D6 D5 D4 D3 D2 D1 D0	02		Focus balance constant (FBAL) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	03		Focus offset constant (FOFS) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	04		Tracking gain constant (TG0) (8-bit mantissa) (1 to 255)	128
D7 D6 D5 D4 D3 D2 D1 D0	05		Tracking gain constant (TEXP0) (8-bit exponent) (16, 32, 64 and 128 only) (Tracking gain constant = mantissa / exponent)	64
D7 D6 D5 D4 D3 D2 D1 D0	06		Tracking balance constant (TBAL) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	07		Tracking offset constant (TOFS) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	16		Disturbance amplitude in focus gain adjustment (FES) (1 to 127)	85
D7 D6 D5 D4 D3 D2 D1 D0	17		Disturbance amplitude in tracking gain adjustment (TES) (1 to 127)	85

(B) Setting of the optical servo characteristics including the characteristics for anti-vibration

・Gain constant

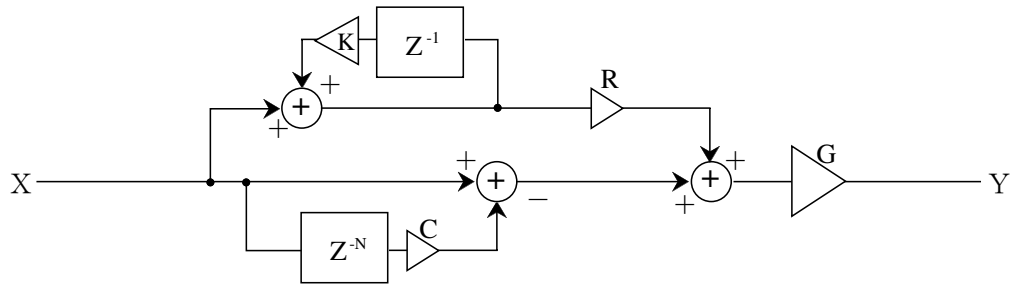
Focus gain mantissa part	FG	Tracking gain mantissa part	TG
Focus gain exponent part	FEXP	Tracking gain exponent part	TEXP

・Phase compensation and low-band compensation constant

Focus phase compensation constant	FC	Tracking phase compensation constant	TC
Focus low-band compensation constant	FR	Tracking low-band compensation constant	TR

The above eight constants can be set by writing 8-bit data (0 to 127) directly with the microcomputer command.

Structure



・f_S of the focus system: 44.1 kHz

・f_S of the tracking system: 44.1 kHz

(f_S of the low-band compensation filter is 22.05 kHz.)

$$G(Z) = G\left\{ \frac{1}{1-Z^{-1}} \times R + (1 - C \times Z^{-N}) \right\}$$

$$G = \frac{TG}{TEXP} \text{ or } \frac{FG}{FEXP} \qquad C = \frac{TC}{128} \text{ or } \frac{FC}{128}$$

$$R = \frac{TR}{2^{15}} \text{ or } \frac{FR}{2^{15}}$$

$K = 1$

N in Z^{-N} can be replaced with :
always 2 in case of the focus system.
1 in case of the tracking system.

・Setting of loop filter constants

Table 7-1-3 (4)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	08	F2	Focus phase compensation constant : FC (8-bit) (1 to 127)	117
D7 D6 D5 D4 D3 D2 D1 D0	09		Focus low-band compensation constant : FR (8-bit) (1 to 127)	64
D7 D6 D5 D4 D3 D2 D1 D0	0A		Tracking phase compensation constant: TC (8-bit) (1 to 127)	122
D7 D6 D5 D4 D3 D2 D1 D0	0B		Tracking low-band compensation constant : TR (8-bit) (1 to 127)	64
D7 D6 D5 D4 D3 D2 D1 D0	0C		Focus phase compensation constant at vibration : FC2 (8-bit) (1 to 127)	117
D7 D6 D5 D4 D3 D2 D1 D0	0D		Focus low-band compensation constant at vibration : FR2 (8-bit) (1 to 127)	64
D7 D6 D5 D4 D3 D2 D1 D0	0E		Tracking phase compensation constant at vibration : TC2 (8-bit) (1 to 127)	122
D7 D6 D5 D4 D3 D2 D1 D0	0F		Tracking low-band compensation constant at vibration : TR2 (8-bit) (1 to 127)	64

(C) Setting of gain crossover for optical servo loop

Before performing focus and tracking automatic adjustments, gain crossover after automatic adjustment can be determined by writing data to the label name GSET (address: 10h) according to the table below.
In the automatic gain adjustment, disturbance is input to the servo loop, and gain is increased or decreased according to the GSET setting after adjusting the gain so that the feedback gain at the frequency becomes 0 dB (gain crossover is equal to the frequency).

(Setting for focus system) Table 7-1-3 (5)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX)	Function (*: Setting at reset)
X X X X D3 D2 D1 D0	10	F2	Focus gain at the frequency set at 750 Hz
X X X X 0 1 1 1			Approx. value : −3.92 dB
X X X X 0 1 1 0			Approx. value : −3.36 dB
X X X X 0 1 0 1			Approx. value : −2.80 dB
X X X X 0 1 0 0			Approx. value : −2.24 dB
X X X X 0 0 1 1			Approx. value : −1.68 dB
X X X X 0 0 1 0			Approx. value : −1.12 dB
X X X X 0 0 0 1			Approx. value : −0.56 dB
X X X X 0 0 0 0			* Approx. value : 0 dB
X X X X 1 1 1 1			Approx. value : 1.05 dB
X X X X 1 1 1 0			Approx. value : 2.11 dB
X X X X 1 1 0 1			Approx. value : 3.16 dB
X X X X 1 1 0 0			Approx. value : 4.21 dB
X X X X 1 0 1 1			Approx. value : 5.27 dB
X X X X 1 0 1 0			Approx. value : 6.32 dB
X X X X 1 0 0 1			Approx. value : 7.37 dB
X X X X 1 0 0 0			Approx. value : 8.43 dB

(Setting for tracking system) Table 7-1-3 (6)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX)	Function (*: Setting at reset)
D7 D6 D5 D4 X X X X	10	F2	Tracking gain at the frequency set at 1 kHz
0 1 1 1 X X X X			Approx. value : −3.92 dB
0 1 1 0 X X X X			Approx. value : −3.36 dB
0 1 0 1 X X X X			Approx. value : −2.80 dB
0 1 0 0 X X X X			Approx. value : −2.24 dB
0 0 1 1 X X X X			Approx. value : −1.68 dB
0 0 1 0 X X X X			Approx. value : −1.12 dB
0 0 0 1 X X X X			Approx. value : −0.56 dB
0 0 0 0 X X X X			* Approx. value : 0 dB
1 1 1 1 X X X X			Approx. value : 1.05 dB
1 1 1 0 X X X X			Approx. value : 2.11 dB
1 1 0 1 X X X X			Approx. value : 3.16 dB
1 1 0 0 X X X X			Approx. value : 4.21 dB
1 0 1 1 X X X X			Approx. value : 5.27 dB
1 0 1 0 X X X X			Approx. value : 6.32 dB
1 0 0 1 X X X X			Approx. value : 7.37 dB
1 0 0 0 X X X X			Approx. value : 8.43 dB

(D) Setting for anti-vibration (VSET)

The gain-up amount and gain-up time can be set when VDET=H.
(VDET can be monitored through the VDETMON pin.)

Table 7-1-3 (7)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
X X X X X D2 D1 D0	11	F2	Setting of the focus gain-up amount at vibration
X X X X X 0 0 0			Scale factor : ×1.0 (0 dB)
X X X X X 0 0 1			Scale factor : ×1.125 (+1.0 dB)
X X X X X 0 1 0			Scale factor : ×1.25 (+1.9 dB)
X X X X X 0 1 1			Scale factor : ×1.375 (+2.8 dB)
X X X X X 1 0 0			* Scale factor : ×1.5 (+3.5 dB)
X X X X X 1 0 1			Scale factor : ×1.625 (+4.2 dB)
X X X X X 1 1 0			Scale factor : ×1.75 (+4.9 dB)
X X X X X 1 1 1			Scale factor : ×2.0 (+6.0 dB)
X X D5 D4 D3 X X X			Setting of the tracking gain-up amount at vibration
X X 0 0 0 X X X			Scale factor : ×1.0 (0 dB)
X X 0 0 1 X X X			Scale factor : ×1.125 (+1.0 dB)
X X 0 1 0 X X X			Scale factor : ×1.25 (+1.9 dB)
X X 0 1 1 X X X			Scale factor : ×1.375 (+2.8 dB)
X X 1 0 0 X X X			Scale factor : ×1.5 (+3.5 dB)
X X 1 0 1 X X X			Scale factor : ×1.625 (+4.2 dB)
X X 1 1 0 X X X			Scale factor : ×1.75 (+4.9 dB)
X X 1 1 1 X X X			* Scale factor : ×2.0 (+6.0 dB)
D7 D6 X X X X X X			Setting of the gain-up time at vibration
0 0 X X X X X X			Time : 23.2 ms
0 1 X X X X X X			Time : 46.4 ms
1 0 X X X X X X			* Time : 92.9 ms
1 1 X X X X X X			Time : 185.8 ms

Note) The gain-up amount set by VSET is valid only when FC2 or FR2 for the focus system or TC2 or TR2 for the tracking system is written after VSET setting.
(No operation is performed to set servo parameters in the anti-vibration mode only by VSET setting.)

The gain values can be overwritten when VDET＝H.

Table 7-1-3 (8)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting values at reset
D7 D6 D5 D4 D3 D2 D1D0	2D	F2	Focus gain constant at vibration (FG2) (8-bit mantissa) (1 to 255)	128
D7 D6 D5 D4 D3 D2 D1D0	2E		Focus gain constant at vibration (FEXP2) (8-bit exponent) (16, 32, 64 and 128 only) (Focus gain constant = mantissa / exponent)	32
D7 D6 D5 D4 D3 D2 D1D0	35		Tracking gain constant at vibration (TG2) (8-bit mantissa) (1 to 255)	128
D7 D6 D5 D4 D3 D2 D1D0	36		Tracking gain constant at vibration (TEXP2) (8-bit exponent) (16, 32, 64 and 128 only) (Tracking gain constant = mantissa / exponent)	64

Note) Be aware that the gain set with VSET applies at the time of fine gain adjustment and writing data to the FC2, FR2, TC2 or TR2.

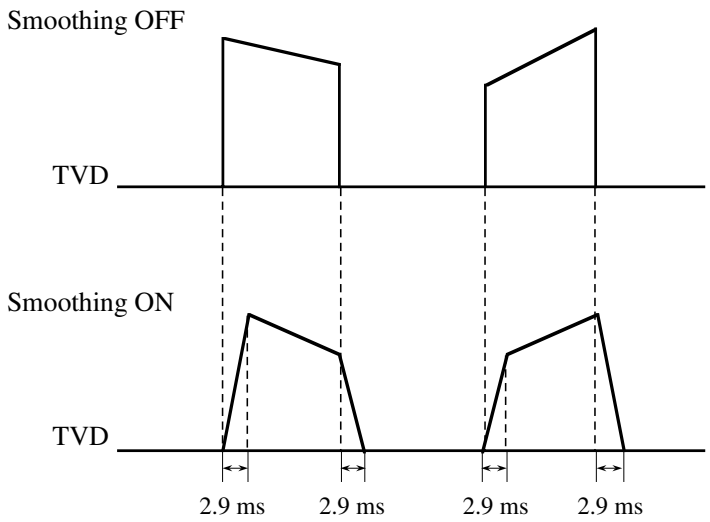
(E) Various system settings

(E)-1 SET0 setting Table 7-1-3 (9)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
D3 D2 X X X X 0 0 0 1 X X X X 0 1 0 1 X X X X 1 0 0 1 X X X X 1 1 0 1	12	F2	Setting of forced brake operation time OFF ON (5.8 ms) * ON (11.6 ms) ON (23.2 ms)
D6 D4 X 0 X 0 X X 0 1 X 0 X 1 X X 0 1 X 1 X 0 X X 0 1 X 1 X 1 X X 0 1			Setting of convergence gain during tracking balance adjustment * ×1/2048 ×1/4096 ×1/1024 ×1/8192
D5 X X 0 X X X 0 1 X X 1 X X X 0 1			Tracking balance adjustment output * As usual Inverted polarity
D7 0 X X X X X 0 1 1 X X X X X 0 1			TVD output smoothing * OFF ON

TVD output

Example of the TVD intermittent drive is as follows.



(E)-2 SET1 setting

Table 7-1-3 (10)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
D0 X X X X X X X 0 X X X X X X X 1	13	F2	TVD output at the time of kick pulse output in the traverse stop condition ＊TVD output No TVD output
D1 X X X X X X 0 X X X X X X X 1 X			Pull-in method when turning focus ON from OFF state ＊ Conventional method High-speed pull-in
D2 X X X X X 0 X X X X X X X 1 X X			High-speed kickback ON/OFF ＊ON OFF
D4 X X X 0 X X X X X X X 1 X X X X			Focus offset adjustment method With vibration ＊Without vibration
D5 X X 0 X X X X X X X 1 X X X X X			Focus offset adjustment method ＊＋direction (Same as MN66271) －direction
D6 D3 X 0 X X 0 X X X X 0 X X 1 X X X X 1 X X 0 X X X X 1 X X 1 X X X			Standby time after TCNT ＊ 50 ms 100 ms 0 ms 10 ms
D7 0 X X X X X X X 1 X X X X X X X			DAC output limiter (FABC, TABC) ＊OFF ON

(E)-3 SET2 setting

Table 7-1-3 (11)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
D1 D0 X X X X X X 0 X X X X X X X 1 0 X X X X X X 1 1	14	F2	Traverse dead-zone amp * Normal (Type A) + side only (Type B) − side only (Type C)
D2 X X X X X 0 X X X X X X X 1 X X			Tracking offset adjustment standby time None * 30 ms
D3 X X X X 0 X X X X X X X 1 X X X			Convergence judgement condition for tracking balance adjustment * ±2 LSBs at TBAL output stage ±1 LSB at TE input stage
D5D4 X X 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1 X X X X			Focus balance adjustment convergence gain * 1/8 1/4 1/32 1/16
D6 X 0 X X X X X X X 1 X X X X X X			Disc detection, focus rough gain adjustment frequency * 5.4 Hz 2.6 Hz
D7 0 X X X X X X X 1 X X X X X X X			Traverse intermittent drive * Output enabled Output disabled

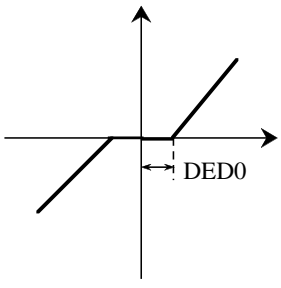


Figure 1 Traverse dead-zone amp Type A

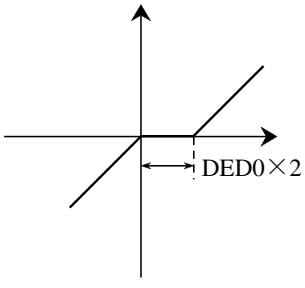


Figure 2 Traverse dead-zone amp Type B

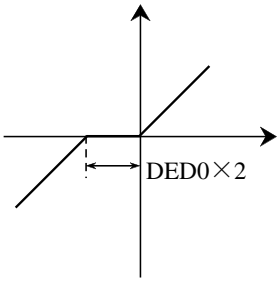


Figure 3 Traverse dead-zone amp Type C

Note) Refer to 7-1 (4) (F)-6 for the DED0 setting.

(E)-4 SET3 setting

Table 7-1-3 (12)

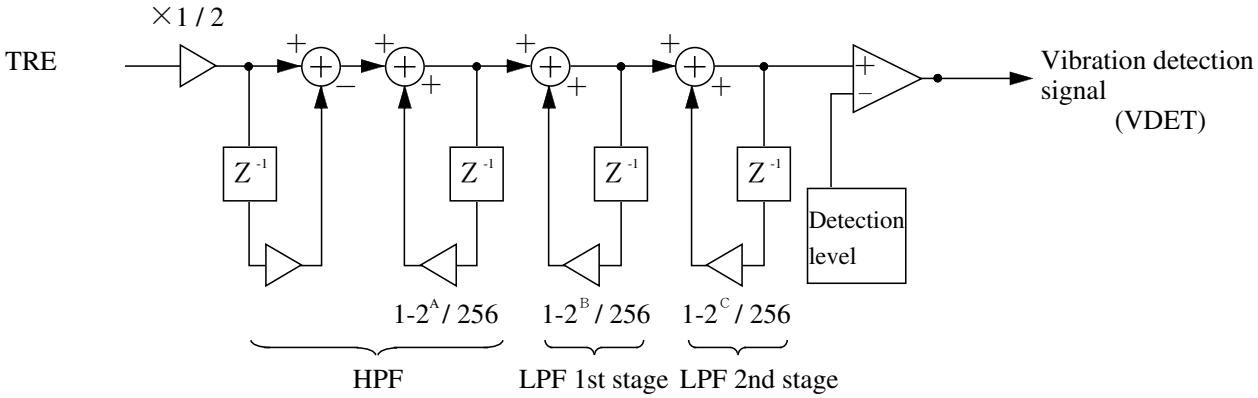
Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
D1 D0 X X X X X X 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1	1E	F2	TVD gain variable * 0 dB (×1.0) 3.5 dB (×1.5) 6.0 dB (×2.0) −2.5 dB (×0.75)
D2 X X X X X 0 X X X X X X X 1 X X			Cancellation of focus balance adjustment * Reset to the initial value at the start of adjustment The adjusting value is on hold
D3 X X X X 0 X X X X X X X 1 X X X			Tracking rough gain adjustment time * 134 ms 319 ms
D4 X X X 0 X X X X X X X 1 X X X X			Focus search mode * As usual Amplitude: 1/4
D5 X X 0 X X X X X X X 1 X X X X X			Offset readjustment after tracking fine gain adjustment * Performed automatically Not performed
D6 X 0 X X X X X X X 1 X X X X X X			Focus balance adjustment output * As usual Inverted polarity
D7 0 X X X X X X X 1 X X X X X X X			Focus search frequency * 1.3 Hz 2.6 Hz

(E)-5 SET5 setting

Table 7-1-3 (13)

(Setting of vibration detection band-pass filter constant)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
D1D0 X X X X X X 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1	15	F2	Setting of LPF 2nd stage constant C 3 4 * 5 6
D3D2 X X X X 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1 X X			Setting of LPF 1st stage constant B 3 4 * 5 6
D5D4 X X 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1 X X X X			Setting of HPF constant A 3 4 * 5 6
D7D6 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1 X X X X X X			Vibration detection level exponent part ×1 ×2 * ×4 ×8 Note) Refer to 7-1 (4) (F)-11 for the setting of mantissa part.



(E)-6 SETTB setting

Table 7-1-3 (14)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
D0 X X X X X X X 0 X X X X X X X 1	4A	F2	Tracking brake damping reinforcement * Damping reinforcement mode 1 Damping reinforcement mode 2
D1 X X X X X X 0 X X X X X X X 1 X			Low-band compensation during tracking brake operation * Yes No
D2 X X X X X 0 X X X X X X X 1 X X			Tracking brake timing * Reference at 1/4-track-before Reference at zero cross
D3 X X X X 0 X X X X X X X 1 X X X			Dropout countermeasure during KICK operation * No Yes
D5 X X 0 X X X X X X X 1 X X X X X			Brake timing countermeasure with OFT noise filter turned on * No Yes
D6 X 0 X X X X X X X 1 X X X X X X			Hunting countermeasure for focus balance adjustment No * Yes
D7 0 X X X X X X X 1 X X X X X X X			Tracking brake noise elimination * Yes No

・Damping Reinforcement

Damping is reinforced by changing the level of KICK pulses, which is set with the KICK2, with servo control turned on in KICK operation.

Mode 1: The inverted pulse in full brake speed control and servo control is set as KICK2.

Mode 2: In addition to the condition in mode 1, the inverted pulse drive after the target track is passed is also set as KICK2.

※ Refer to 7-1 (4) (F)-9 for the KICK pulse level setting.

(E)-7 Software reset

The servo processing is initialized if data of AAh address is accessed. DSP processing starts with the first address.

Table 7-1-3 (15)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
X X X X X X X X	AA	F2	Software reset (Data is disabled.)

(E)-8 Forced gain-up setting

The LSI can be in forced gain-up mode by accessing the data of 81h address.
This mode is reset by accessing the data in 80h address.

Table 7-1-3 (16)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (*: Setting at reset)
X X X X X X X X	81	F2	Focus / tracking forced gain-up (Data is disabled.)
X X X X X X X X	80		Focus / tracking normal gain (Data is disabled.)

Note) ・The VDET monitor signal is not set to H when the forced gain-up command is issued.
・The status of the VDET can be monitored through the VDETMON pin.
・The output of the VDETMON pin varies from H to L when vibration is detected even in the forced gain-up mode. Then, this mode is not reset.

(F) Optical servo system setting

(F)-1 Focus search setting Table 7-1-3 (17)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	18	F2	Focus search amplitude (CRAM2) setting 8-bit data (p-p) (40 to 127)	45
D0	19		Focus search/disc detection direction (SD) setting 8-bit data (0, 1) (0: Reducing FOD)	0

Note 1) In focus search/disc detection direction setting, a value of SD will change automatically according to execution of a focus search/disc detection. Consequently, the values written by initial setting and DTMS may have changed when they are read out with DTSM. If you want to perform a focus search/disc detection from the same direction every time, it is necessary to set with DTMS every time before the focus search/disc detection.
To make SD settings, check the SD value with the DTSM so that no bit values other than the set bit value will change.

(F)-2 Setting of tracking servo fail-safe value (CRAM3) Table 7-1-3 (18)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	1C	F2	Fail-safe value clip level 8-bit data (0 to 127) Low-band component of drive output in the tracking brake mode is clipped at the specified value.	72

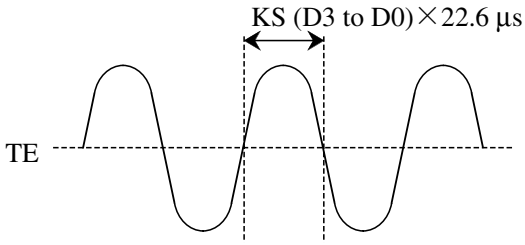
(F)-3 Setting of disturbance amplitude (CRAM4) in tracking balance adjustment Table 7-1-3 (19)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	1D	F2	Disturbance amplitude (one side) 8-bit data (0 to 127) Amplitude of the disturbance waves input in the tracking balance adjustment is set. Actual disturbance amplitude is 1/8×CRAM4.	72

(F)-4 KICK setting Table 7-1-3 (20)

Data (8 bits)	Address (8 bits)	Command (8 bits)	Function	Setting values at reset
X X X X D3 D2 D1 D0	1A	F2	KICK speed (KS) setting 4-bit data (6 to 15)	6
D7 D6 D5 D4 X X X X			KICK brake timing setting 4-bit data (0 to 15)	0

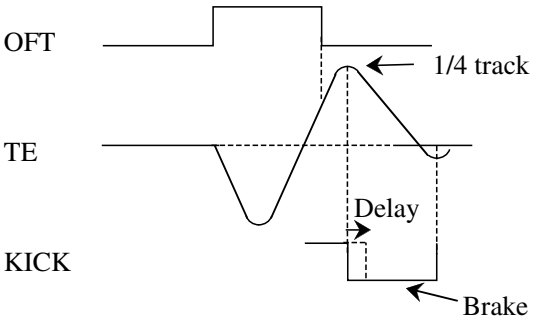
・TE cycle in the speed control mode is determined by the KICK speed setting.



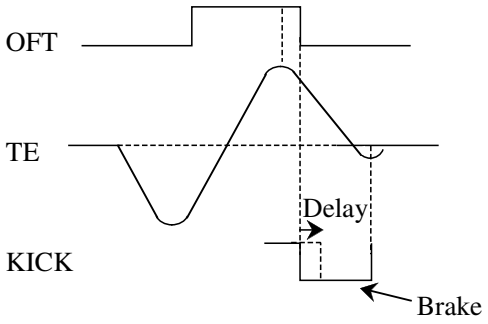
・KICK brake output timing delay time is set in the KICK brake timing setting.
(1 count=22.6 µs delay) Setting value=0: No delay

〔1/4-track-before Brake Mode〕 SETTB (address: 4Ah) D2=0

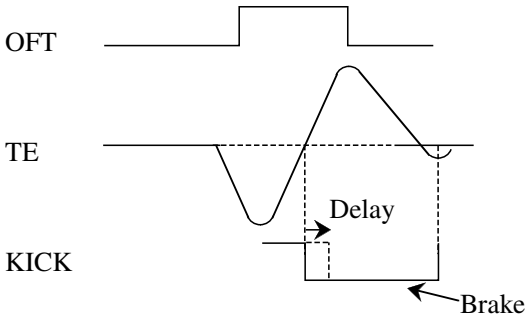
① When OFT is turned to "L" before reaching a position of 1/4 track



② When OFT is turned to "L" after passing the position of 1/4 track



〔Zero Cross Brake Mode〕 SETTB (address: 4Ah) D2=1



(F)-5 Traverse drive constant in tracking brake (TVG) Table 7-1-3 (21)

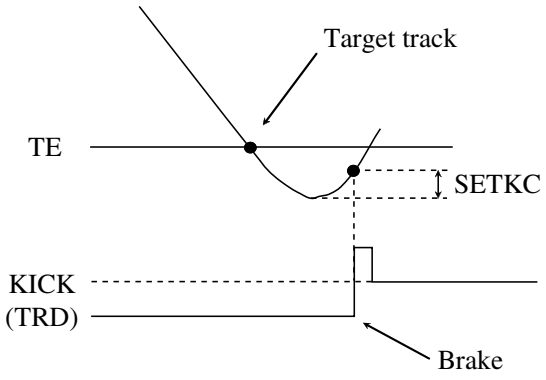
Data (8 bits)	Address (8 bits)	Command (8 bits)	Function	Setting at reset
X X X X D3 D2 D1 D0	1B	F2	Traverse drive constant TVG (1 to 15) Only in the tracking brake, traverse will be driven with the traverse error multiplied by the required constant.	2

(F)-6 Traverse drive dead zone setting (DED0) Table 7-1-3 (22)

Data (8 bits)	Address (8 bits)	Command (8 bits)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	1F	F2	Traverse drive dead zone setting (one side) DED0 (0 to 127)	24

(F)-7 TE noise elimination width setting at track count/kick (SETKC) Table 7-1-3 (23)

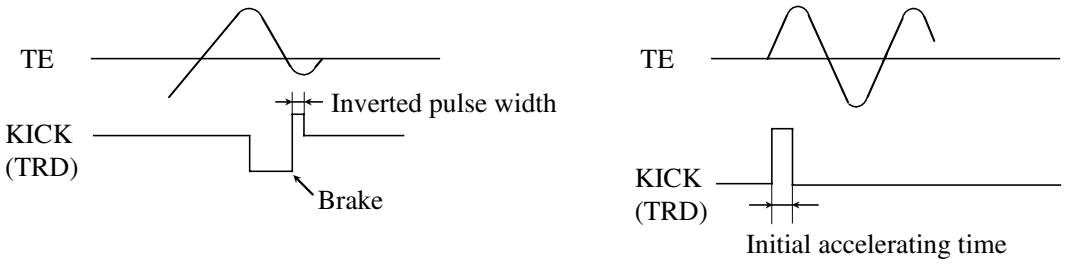
Data (8 bits)	Address (8 bits)	Command (8 bits)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	49	F2	TE noise elimination width setting at track counting/kick SETKC (0 to 127)	3



※ When the TE gradient is inverted and reaches the level of the SETKC, braking completes.

(F)-8 KICK pulse width setting (KCCNT) Table 7-1-3 (24)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 X X X X	4B	F2	Inverted pulse width during servo pull-in operation in KICK operation. (Set value×22.6+11.3) µs	1
X X X X D3 D2 D1 D0			KICK pulse initial accelerating time (0 to 15) (Set value×22.6) µs	5



(F)-9 KICK pulse level setting (KICK and KICK2) Table 7-1-3 (25)

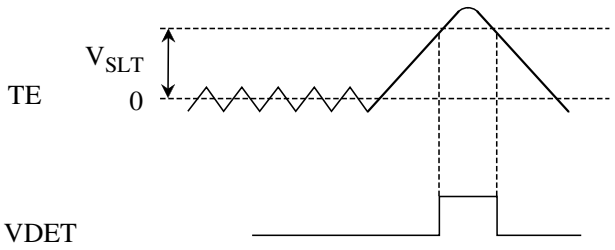
Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	78	F2	Setting KICK pulse level in normal operation KICK (0 to 127)	84
0 D6 D5 D4 D3 D2 D1 D0	7A		Setting KICK pulse level during servo pull-in operation KICK2 (0 to 127)	84

(F)-10 Traverse output gain setting (TRV) Table 7-1-3 (26)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	79	F2	Traverse output gain setting TRV (0 to 127)	95

(F)-11 VDET detecting level setting Table 7-1-3 (27)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	7B	F2	VDET detection TE threshold level setting (mantissa part) V_{SLT} (1 to 255)	57



Threshold level exponent part
(Refer to 7-1 (4) (E)-5.)
SET5 [D7, D6] threshold level

〔0, 0〕 : $\pm V_{SLT} \times 1$
〔0, 1〕 : $\pm V_{SLT} \times 2$
〔1, 0〕 : $\pm V_{SLT} \times 4$
〔1, 1〕 : $\pm V_{SLT} \times 8$

(F)-12 Number of disturbance waves in fine gain adjustment (PHSU) Table 7-1-3 (28)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	7C	F2	Number of disturbance waves in fine gain adjustment (See Note.) PHSU (1 to 255)	129

Note) The convergence gain increases as the number of disturbance waves increases.

(F)-13 Setting of convergence gain in fine gain adjustment (PDK) Table 7-1-3 (29)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
X X X X X D2 D1 D0	61	F2	Convergence gain in Fo fine gain adjustment	66
X X X X X 0 0 0			× 1	
X X X X X 0 0 1			× 2	
X X X X X 0 1 0			* × 4	
X X X X X 0 1 1			× 8	
X X X X X 1 0 0			× 16	
X X X X X 1 0 1			× 32	
X X X X X 1 1 0			× 64	
X X X X X 1 1 1			×128	
D7 D6 D5 X X X X X			Convergence gain in Tr fine gain adjustment	
0 0 0 X X X X X			× 1	
0 0 1 X X X X X			× 2	
0 1 0 X X X X X			* × 4	
0 1 1 X X X X X			× 8	
1 0 0 X X X X X			× 16	
1 0 1 X X X X X			× 32	
1 1 0 X X X X X			× 64	
1 1 1 X X X X X			×128	

(F)-14 Setting of automatic adjustment range

The limits of adjustment values can be set arbitrarily in the range of 1/128 to 255/16 (or −42 dB to +24 dB). In order to ensure automatic gain convergence within a limited, narrow adjustment range to prevent excessive gain change, which has difficulty in convergence control, however, make sure that the maximum automatic adjustment range is ±9 dB on the basis of the gain set value.

・Tracking gain
Automatic adjustment range GLT3/GLT4 to GLT1/GLT2

Table 7-1-3 (30)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	3D	F2	Tracking gain upper limit GLT1 (mantissa) (128 to 255)	181
D7 D6 D5 D4 D3 D2 D1 D0	3E		GLT2 (exponent) (128, 64, 32, 16)	32
D7 D6 D5 D4 D3 D2 D1 D0	3F		Tracking gain lower limit GLT3 (mantissa) (128 to 255)	91
D7 D6 D5 D4 D3 D2 D1 D0	40		GLT4 (exponent) (128, 64, 32, 16)	128

GLT1 and GLT3 can be both set to 127 or a smaller value only if GLT2 and GLT4 are both set to 128.

・Focus gain
Automatic adjustment range GLF3/GLF4 to GLF1/GLF2

Table 7-1-3 (31)

Data (8 bits)	Address (8 bits)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	39	F2	Focus gain upper limit GLF1 (mantissa) (128 to 255)	181
D7 D6 D5 D4 D3 D2 D1 D0	3A		GLF2 (exponent) (128, 64, 32, 16)	16
D7 D6 D5 D4 D3 D2 D1 D0	3B		Focus gain lower limit GLF3 (mantissa) (128 to 255)	181
D7 D6 D5 D4 D3 D2 D1 D0	3C		GLF4 (exponent) (128, 64, 32, 16)	128

GLF1 and GLF3 can be both set to 127 or a smaller value only if GLF2 and GLF4 are both set to 128.

[3] Access command setting

Table 7-1-3 (32)

Data (16 bits)	Command (8 bits)	Function
D15 0 0 0 0 0 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 0 0 0 0 0 0 1 0 0 0 0 0 KICK-count setting (other than 0)	1 1 1 1 0 0 0 1	KICK-count setting/KICK operation start Inner track KICK operation Outer track KICK operation
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 0 1 Track-count setting	1 1 1 1 0 0 1 1	Track-count setting / Track counting start Inner track counting Outer track counting

Note) The track-count means the number of tracks until the brake operation start point is reached.

7-1 (4) Data setting in signal processing section

(A) Audio output control (I)

Table 7-1-4 (1)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X X X X X X X X X X D1 D0	0 1 0 0 0 0 0 1	Available for bilingual
X X X X X X X X X X X X X X 0 0		* Normal stereo
X X X X X X X X X X X X X X 0 1		L-ch monaural
X X X X X X X X X X X X X X 1 0		R-ch monaural
X X X X X X X X X X X X X X 1 1		L-/R-ch reverse
X X X X X X X X X X X X X D2 X X		D/A converter output polarity
X X X X X X X X X X X X X 0 X X		* Normal
X X X X X X X X X X X X X 1 X X		Inverse
X X X X X X X X X X X D4 D3 X X X		Emphasis control
X X X X X X X X X X X 0 X X X X		* Control by DEMPH output
X X X X X X X X X X X 1 0 X X X		Forced OFF
X X X X X X X X X X X 1 1 X X X		Forced ON
X X X X X X X X X D6 D5 X X X X X		Peak detection
X X X X X X X X X X 0 X X X X X		* L-ch, R-ch
X X X X X X X X X 0 1 X X X X X		L-ch
X X X X X X X X X 1 1 X X X X X		R-ch
X X X X X X X X D7 X X X X X X X X		CLV synchronization stabilized status detection flag control
X X X X X X X X 0 X X X X X X X X		* Accepted at 64 counts of IPFLAG
X X X X X X X X 1 X X X X X X X X		Accepted at 32 counts of IPFLAG
X X X X X X D9 X X X X X X X X X X		SRDATA de-emphasis control
X X X X X X 0 X X X X X X X X X X		* Not controlled
X X X X X X 1 X X X X X X X X X X		Controlled
X X X X D11 D10 X X X X X X X X X X		CD-TEXT control
X X X X 0 0 X X X X X X X X X X		* Not controlled
X X X X 0 1 X X X X X X X X X X		CD-TEXT mode 1
X X X X 1 0 X X X X X X X X X X		CD-TEXT mode 2
X X X X 1 1 X X X X X X X X X X		CD-TEXT mode 3
X X X D12 X X X X X X X X X X X X		CD-TEXT CRC operation control
X X X 0 X X X X X X X X X X X X		* CRC operation result output
X X X 1 X X X X X X X X X X X X		TEXT data position flag output in BLKCK
X X D13 X X X X X X X X X X X X X		TEXT data output byte control in CD-TEXT mode 3
X X 0 X X X X X X X X X X X X X		* TEXT data 16-byte output
X X 1 X X X X X X X X X X X X X		TEXT data 18-byte output
D15 X X X X X X X X X X X X X X X		CD-TEXT mode 4 control
0 X X X X X X X X X X X X X X X		* Not controlled
1 X X X X X X X X X X X X X X X		CD-TEXT mode 4

(B) Digital audio interface control

Table 7-1-4 (2)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X X X X X X X D3 X D1 D0 X X X X X X X X X X X 0 X 0 0 X X X X X X X X X X X 0 X 1 0 X X X X X X X X X X X 0 X 1 1 X X X X X X X X X X X 1 X X X	0 1 0 0 0 0 1 0	Bit U control of TX output * LDON control Bit U enabled Bit U fixed to "H" Mute control (Bit U is fixed to "H" with DMUTE pin set to "H" or with SRDATA mute command.)
X X X X X X X X X X X X D2 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X		Generation status bit control of TX output * Generation status bit 0 Generation status bit 1
X X X X X X X X X X D4 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X		TX mute control * Mute OFF Mute ON
X X X X X X X X X D5 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X X		TX Bit V mode selection (during interpolation) * Bit V is ON Bit V is not ON
X X X X X X X X D6 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X X X		TX data selection * DF input data As usual
X X X X X X X D7 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X X X X		TX Bit V mode selection (during ATT) * Bit V is ON Bit V is not ON

(C) General-purpose I/O port control

The general-purpose I/O port has four pins, which are GIO0 through GIO3 pins. The default settings of the GIO0 and GIO3 pins are for the input signals SQCK and RSEL of the LSI respectively.

Command execution makes it possible to make general-purpose I/O port settings of the GIO0 and GIO3 pins.

Unlike the GIO0 and GIO3 pins, the GIO1 and GIO2 pins work as output ports at the time of LSI resetting. The GIO1 and GIO2 pins have low-level output.

Command execution makes it possible to make general-purpose I/O port settings and ~~CLDCK~~ and FCLK output signal settings of the LSI.

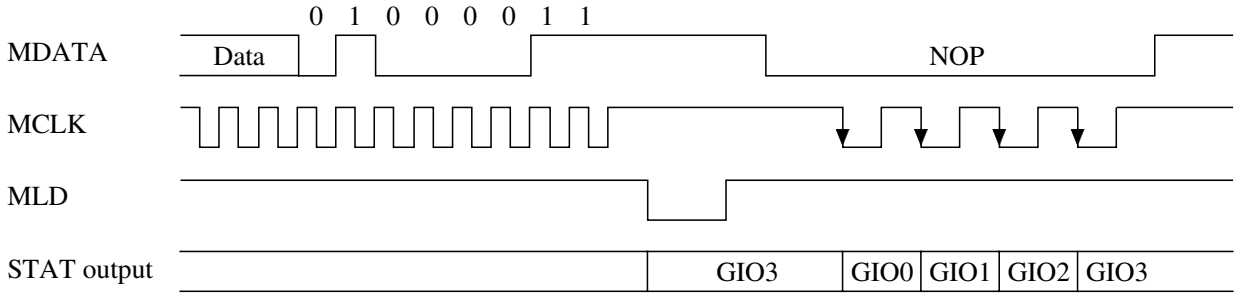
Note) Do not apply middle-level input if these pins are used as general-purpose input ports.

Table 7-1-4 (3)

Data (16 bits)																Address (8 bits)	Function (*: Setting at reset)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0 1 0 0 0 0 1 1	
X	X	X	X	0	1	1	0	0	1	1	0	X	X	X	X		* Default setting
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0		Port output value setting 0: Output value at "L"
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1		1: Output value at "H" (Enabled when the port is set as output port.)
													D2	D1			Port designation address
X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X		GIO0 designation
X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X		GIO1 designation
X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X		GIO2 designation
X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X		GIO3 designation
												D3					Port output value setting enabled or disabled
X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X		Port output value setting disabled
X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X		Port output value setting enabled
								D7	D6	D5	D4						Port I/O mode setting
X	X	X	X	X	X	X	X	GIO3	GIO2	GIO1	GIO0	X	X	X	X		0: Input port 1: Output port
				D11	D10	D9	D8										Function selection mode setting
X	X	X	X	GIO3	GIO2	GIO1	GIO0	X	X	X	X	X	X	X	X		0: LSI I/O mode 1: General-purpose I/O port mode
D15																	Mode setting enabled or disabled
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		0: I/O mode setting and function selection mode setting disabled
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		1: I/O mode setting and function selection mode setting enabled
	D14																RF signal polarity control
X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X		RF polarity bright level "L"
X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X		* RF polarity bright level "H"

If D15 disables mode setting, the command is disabled except the port output signal level setting data. Therefore, changes in the output signal level are made with ease.

After all settings, the input signals (or output signals if the port is so set) of the GIO3 through GIO0 pins are output from the STAT pin in series. The signals are output in synchronization with the falling edge of the MCLK as shown in the following timing chart.



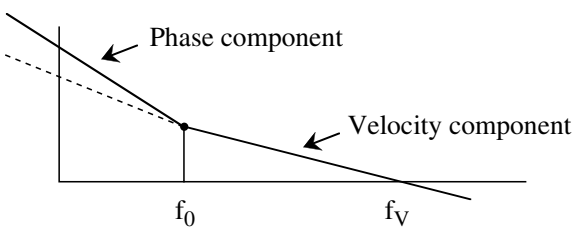
General-purpose I/O port output timing

(D) Spindle control

Table 7-1-4 (4)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X D10 X X X X X D4 X X X D0 X X X X X 0 X X X X X 0 X X X 0 X X X X X 0 X X X X X 0 X X X 1 X X X X X 0 X X X X X 1 X X X 0 X X X X X 0 X X X X X 1 X X X 1	0 1 0 0 0 1 0 1	f_0 frequency setting * f_0 = 24 Hz f_0 = 6 Hz f_0 = 12 Hz f_0 = 3 Hz
X X X X X D10 X X X X X X X D2 D1 X X X X X X 0 X X X X X X X 0 0 X X X X X X 0 X X X X X X X 0 1 X X X X X X 0 X X X X X X X 1 0 X X X X X X 0 X X X X X X X 1 1 X		Spindle gain setting * Normal gain Gain + 6 dB Gain +12 dB Gain − 6 dB
X X X X X D10 X X X X X X D3 X X X X X X X X 0 X X X X X X 0 X X X X X X X X 0 X X X X X X 1 X X X		4x-speed playback mode setting * 4x-speed playback mode canceled 4x-speed playback mode setting
X X X X X D10 X X D7 X X X X X X X X X X X X 0 X X 0 X X X X X X X X X X X X 0 X X 1 X X X X X X X		SRF/EFM input selection * SRF input EFM input
X X X X X D10 X D8 X X X X X X X X X X X X X 0 X 0 X X X X X X X X X X X X X 0 X 1 X X X X X X X X		PC pin polarity setting * When spindle monitor output is ON, PC pin=L. When spindle monitor output is ON, PC pin=H.
X X X X D11 D10 X X X X X X X X X X X X X 0 0 X X X X X X X X X X X X X 1 0 X X X X X X X X X		Jitter-free mode * OFF ON
X X X D12 X D10 X X X X X X X X X X X X 0 X 0 X X X X X X X X X X X X 1 X 0 X X X X X X X X X		PLL phase comparison output (PLLF) * ON OFF (Only when tracking is OFF)
X X D13 X X D10 X X X X X X X X X X X 0 X X 0 X X X X X X X X X X X 1 X X 0 X X X X X X X X X		STAT output selection * OFF (Normal) ON (FCLV→RESY)
X D14 X X X D10 X X X X X X X X X X 0 X X X 0 X X X X X X X X X X 1 X X X 0 X X X X X X X X X		Power-down mode setting * Normal mode Power-down mode (DF/DAC clock stopped)

Note) f_0 frequency:
Considering the gain crossover point to be f_V, the point shown on the right is described as f_0.



(E) Audio output control (II)

Table 7-1-4 (5)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X X X X X X X X X X X D0 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1	0 1 0 0 0 1 1 0	Correction CPU reset control * Not controlled Reset
X X X X X X X X D6 X X X D2 D1 X X X X X X X X X 0 X X X 0 0 X X X X X X X X X 1 X X X 1 1 X		C2 correction selection * C2 triple correction C2 quadruple correction
X X X X X X X X X X X X D3 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X		$\overline{\text{CLDCK}}$ output duty control * Normal 50 % output duty
X X X X X X X X X X X D4 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X		SRDATA attenuation control * Not controlled Attenuation (−12 dB)
X X X X X X X X X X D5 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X		PCK and EFM output control * Normal output PCK and EFM output fixed to L
X X X X X X X X D7 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X		CK384 control (at IOSEL=L) * CK384 output (Xtal) 384f_S output for signal processing (VCO output in jitter-free mode)
X X X X X X X D8 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X		Spindle gain-down * No gain-down −3.5 dB (One per three ECS outputs is not output.)
X X X X X X D9 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X		EDATA flag selection * FLAG0 IPFLAG
X X X X X D10 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X X X X X X		Serial data mute control * Mute OFF Mute ON
X X X X D11 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X X X X X X X		DF/DAC output mute * Mute OFF Mute ON
X X X D12 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X X X X X X X X		PLL pull-in mode selection * 12T detection output width: 64 PCK 12T detection output width: 32 PCK

Note) Set the C2 correction selection to the triple correction mode for audio CD playback.

Note) When using C2 quadruple correction, set the selection (2T or 5T) of 4Dh command PLL detection to 2T.

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X D14 D13 X X X X X X X X X X X X X X 0 0 X X X X X X X X X X X X X X 0 1 X X X X X X X X X X X X X X 1 0 X X X X X X X X X X X X X X 1 1 X X X X X X X X X X X X X	0 1 0 0 0 1 1 0	PLLF2 pin control (on-chip switch) * Forced OFF Forced ON ON with RESY set to "H" ON with RESY set to "L"
D15 X X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X X X X		PCK pin output mode * PLL clock output DSL balance output

(F) Audio output control (III)

Table 7-1-4 (6)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X D11 X X X X X D5 X X X X D0 X X X X 0 X X X X X 0 X X X X 0 X X X X 0 X X X X X 0 X X X X 1	0 1 0 0 0 1 1 1	$\overline{\text{RFDET}}$ processing control of servo CPU * $\overline{\text{RFDET}}$ normal processing Data processed as L-level signal regardless of input
X X X X D11 X X X X X D5 X X X D1 X X X X X 0 X X X X X 0 X X X 0 X X X X X 0 X X X X X 0 X X X 1 X		STAT output selection (with output selected with MCLK) * OFF (Normal) ON ($\overline{\text{FLOCK}}$ → $\overline{\text{RFDET}}$)
X X X X D11 X X X X X D5 X X D2 X X X X X X 0 X X X X X X X X 0 X X X X X X 0 X X X X X X X X 1 X X		DSLBDA pin output mode * Not controlled DSLB DAC output
X X X X D11 X X X X X D5 X D3 X X X X X X X 0 X X X X X 0 X 0 X X X X X X X 0 X X X X X 0 X 1 X X X		SUBQ output control (SSEL=H) * MSB-first output LSB-first output in the unit of byte
X X X X D11 X X X X X D5 D4 X X X X X X X X 0 X X X X X 0 0 X X X X X X X X 0 X X X X X 0 1 X X X X		Oscillation stop control (See Note.) * Normal Oscillation stop
X X X X D11 X X X X D6 D5 X X X X X X X X X 0 X X X X 0 0 X X X X X X X X X 0 X X X X 1 0 X X X X X		DSL balance compensation circuit setting * Operation stop (with output on hold) Compensation value retrieval
X X X X D11 X X X D7 X D5 X X X X X X X X X 0 X X X 0 X 0 X X X X X X X X X 0 X X X 1 X 0 X X X X X		TRV pin intermittent drive control * Normal mode (continuous drive) Intermittent drive (at 44.1 kHz)
X X X X D11 X X D8 X X D5 X X X X X X X X X 0 X X 0 X X 0 X X X X X X X X X 0 X X 1 X X 0 X X X X X		DSL offset function with Tr OFF * With DSL offset With no DSL offset
X X X X D11 X D9 X X X D5 X X X X X X X X X 0 X 0 X X X 0 X X X X X X X X X 0 X 1 X X X 0 X X X X X		LSI clock control * Clock enabled Clock disabled
X X X X D11 D10 X X X X D5 X X X X X X X X X 0 0 X X X X 0 X X X X X X X X X 0 1 X X X X 0 X X X X X		Power down control * Not controlled VCO, A/D, DF/DAC disabled

Note) Oscillation stop control can be reset with $\overline{\text{RST}}$.

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X D13 D12 D11 X X X X X D5 X X X X X X X 0 0 0 X X X X X 0 X X X X X X X 0 1 0 X X X X X 0 X X X X X X X 1 1 0 X X X X X 0 X X X X X	0 1 0 0 0 1 1 1	Track cross operation control * Not controlled Noise elimination at 4 MHz Noise elimination at 2 MHz
X D14 X X D11 X X X X X D5 X X X X X X 0 X X 0 X X X X X 0 X X X X X X 1 X X 0 X X X X X 0 X X X X X		KICK pulse width control * Not controlled Controlled

(G) CLV speed setting

Table 7-1-4 (7)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X X D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 X X X X X X 0 0 0 0 0 0 0 0 0 0 X X X X X X 0 0 1 0 0 0 0 0 0 0 X X X X X X 1 1 0 1 1 1 1 1 1 1	0 1 0 0 1 0 0 1	Setting of variable pitch data (D9 to D0) * 0 % +51.1 % (maximum value) −51.2 % (minimum value)
X X X X X D10 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X X		Variable pitch selection * Variable pitch OFF Variable pitch ON
X X X X D11 X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X 1 X X X X X X X X X X		ON/OFF setting of VCO oscillation for variable pitch control (See Note.) * VCO oscillation OFF VCO oscillation ON
X X X X D11 X X X D7 D6 D5 D4 D3 D2 D1 D0 X X X X 1 X X X D7 D6 D5 D4 D3 D2 D1 D0		Disc rotation speed judgement data setting (in jitter-free mode) 8-bit data
X X X D12 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X		DF/DAC clock lock setting * Normal Locked
X X D13 X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X X		VCO charge pump current source control * Current ON Current OFF

Note) In jitter-free mode, turn VCO on.

(H) DSL and PLL control (I)

Table 7-1-4 (8)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X X X X X X X X X X D1 D0	0 1 0 0 1 0 1 1	PLLF current selection
X X X X X X X X X X X X X X 0 0		* ×1
X X X X X X X X X X X X X X 0 1		×1.25
X X X X X X X X X X X X X X 1 0		×0.5
X X X X X X X X X X X X X X 1 1		×0.75
X X X X X X X X X X X X D3 D2 X X		PLLF current selection (Linked with value
X X X X X X X X X X X X 0 0 X X		* ×1 set in D1 and D0)
X X X X X X X X X X X X 0 1 X X		×1.25
X X X X X X X X X X X X 1 0 X X		×0.5
X X X X X X X X X X X X 1 1 X X		×0.75
X X X X X X X X X X D5 D4 X X X X		OFT noise filter control
X X X X X X X X X X 0 0 X X X X		* Not controlled
X X X X X X X X X X 0 1 X X X X		Control mode 1
X X X X X X X X X X 1 X X X X X		Control mode 2
X X X X X X X X X D6 X X X X X X		VCO control
X X X X X X X X X 0 X X X X X X		* Pitch control and servo VCO operation
X X X X X X X X X 1 X X X X X X		VCO stopped
X X X X X X X X D7 X X X X X X X		PLL frequency-dividing control (See Note.)
X X X X X X X X 0 X X X X X X X		* Not controlled
X X X X X X X X 1 X X X X X X X		Controlled

D6 of address 4Bh and D11 of address 49h are available to a command each for controlling the VCO for pitch control and/or that for servo use. Refer to the following for available control modes according to the command.

4Bh D6 (VCO control)	49h D11 (Pitch control VCO oscillation)	Pitch control VCO	Servo VCO
0	–	Oscillation	Oscillation
1	0	Stop	Stop
1	1	Oscillation	Stop

Note) In principle, set the bit to 1 to enable PLL frequency-dividing control.

(I) DSL and PLL control (II)

Table 7-1-4 (9)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X X X X X X X D3 X D1 D0	0 1 0 0 1 1 0 1	Dropout operation (CLV) (PLL) (DSL)
0 0 0 0 0 0 0 X X X X X 0 X 0 0		* Enable Enable Enable
0 0 0 0 0 0 0 X X X X X X X X 1		— — Stop
0 0 0 0 0 0 0 X X X X X X X 1 X		— Stop —
0 0 0 0 0 0 0 X X X X X 1 X X X		Stop — —
0 0 0 0 0 0 0 X X X X X X D2 X X		PLL gain control
0 0 0 0 0 0 0 X X X X X X 0 X X		* Normal mode (Tracking OFF→Gain-up at ON)
0 0 0 0 0 0 0 X X X X X X 1 X X		Gain-up mode
0 0 0 0 0 0 0 X X X X D4 X X X X		PLL 2T or 5T detection selection
0 0 0 0 0 0 0 X X X X 0 X X X X		2T
0 0 0 0 0 0 0 X X X X 1 X X X X		* 5T
0 0 0 0 0 0 0 D8 D7 D6 D5 X X X X X		PLL pull-in mode selection
0 0 0 0 0 0 0 0 0 0 0 X X X X X		* 2T and 5T detecting output width
0 0 0 0 0 0 0 1 1 0 1 X X X X X		32 PCK
0 0 0 0 0 0 0 1 0 1 1 X X X X X		44 PCK
0 0 0 0 0 0 0 1 0 0 0 X X X X X		52 PCK
		64 PCK

Note) The following formula is available for setting 2T and 5T detecting output widths.
2T or 5T detecting output width = $D8 \times 32 + \overline{D7} \times 16 + \overline{D6} \times 8 + \overline{D5} \times 4 + 4$

Note) When using C2 quadruple correction, set the selection (2T or 5T) of 4Dh command PLL detection to 2T.

(J) DIGTAL PLL control

Table 7-1-4 (10)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
X X X X X X X X X X X X D2 D1 D0 X X X X X X X X X X X X 0 0 0 ⋮ X X X X X X X X X X X X 1 1 1	0 1 0 0 1 1 1 0	Increment/Decrement counter limit setting ＊ Limit value 14 (See Note.) ⋮ Limit value 0
X X X X X X X X X X X X D3 X X X		Increment/Decrement counter clear mode setting
X X X X X X X X X X X X 0 X X X		＊ 1/2
X X X X X X X X X X X X 1 X X X		Cleared to be 0.
X X X X X X X X X D5 D4 X X X X		PCK delay value setting
X X X X X X X X X 0 0 X X X X		＊ PCK delay 0
X X X X X X X X X 0 1 X X X X		PCK delay 1 clock
X X X X X X X X X 1 0 X X X X		PCK delay 2 clock
X X X X X X X X X 1 1 X X X X		PCK delay 3 clock
X X X X X X X X D6 X X X X X X		Resolution selection
X X X X X X X X 0 X X X X X X		＊ 1/8
X X X X X X X X 1 X X X X X X		1/16
X X X X X X X D7 X X X X X X X		VCO oscillation frequency selection
X X X X X X X 0 X X X X X X X		＊ 67 MHz
X X X X X X X 1 X X X X X X X		138 MHz
X X X X X X D8 X X X X X X X X		PCK generation PLL selection
X X X X X X 0 X X X X X X X X		＊ Analog PLL
X X X X X X 1 X X X X X X X X		Digital PLL
X X X X X D9 X X X X X X X X X		VCO selection
X X X X X 0 X X X X X X X X X		＊ Pitch control and jitter-free
X X X X X 1 X X X X X X X X X		Digital PLL
X X X X D10 X X X X X X X X X X		Digital PLL operating frequency setting
X X X X 0 X X X X X X X X X X		＊ Normal
X X X X 1 X X X X X X X X X X		×2

Note) Limit value＝$8\times\overline{D2}+4\times\overline{D1}+2\times\overline{D0}$

When the VCO is set to digital PLL use (i.e., D9 of the above command is set to 1), pitch control or jitter-free function is not available.

(K) STAT pin control

Table 7-1-4 (11)

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
Unnecessary for this command (8 bits) X X X X X X X X X X X X X X X X	0 1 1 1 0 0 0 0	STAT pin output : CRC
X X X X X X X X X X X X X X X X	0 1 1 1 0 0 0 1	: STCNT
X X X X X X X X X X X X X X X X	0 1 1 1 0 0 1 0	: CLVS
X X X X X X X X X X X X X X X X	0 1 1 1 0 0 1 1	: TTSTOP (TTOFF) JCLVS (TTON)
X X X X X X X X X X X X X X X X	0 1 1 1 0 1 0 0	: SQOK
X X X X X X X X X X X X X X X X	0 1 1 1 0 1 1 1	: FCLV
X X X X X X X X X X X X X X X X	0 1 1 1 1 0 0 0	: SUBQ
X X X X X X X X X X X X X X X X	0 1 1 1 1 0 0 1	: SYFLG
X X X X X X X X X X X X X X X X	0 1 1 1 1 0 1 0	: EDATA
X X X X X X X X X X X X X D2 D1 X	0 1 1 1 0 1 0 1	STAT pin output setting STAT pin output : FLAG6
X X X X X X X X X X X X X 0 0 X		: SENSE
X X X X X X X X X X X X X 0 1 X		: $\overline{\text{FLOCK}}$ (RFDET)
X X X X X X X X X X X X X 1 0 X		: $\overline{\text{TLOCK}}$
X X X X X X X X X X X X X 1 1 X		
X X X X X X X X X X X X X X X D0		Control of FLAG6 output from STAT pin
X X X X X X X X X X X X X X X 0		NOP
X X X X X X X X X X X X X X X 1		Reset of FLAG6
0 0 0 0 0 0 0 0 D7 0 0 0 0 0 0 0	0 1 1 1 0 1 1 0	Disc rotation speed data output from STAT pin
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		* Frame memory address reset OFF
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0		Frame memory address reset ON

7-1 (5) Automatic adjustment

Following is a list of automatic adjustment.

Table 7-1-5

	Command								Description	Time required	Traverse operation
	B7	B6	B5	B4	B3	B2	B1	B0			
Fo/Tr offset AOC	1	1	1	1	1	0	0	1	Averages and corrects the focus error values and tracking error values as offset when the laser is turned on or off.	50 ms to 140 ms	FWD/ REV enabled
Fo balance ABC1	1	1	1	1	0	1	1	1	Inputs the disturbance into the focus servo loop, and make corrections so that the envelope ripple for the 3T component of the RF signal in the positive and negative parts of the FE signal should be balanced. The output pin for corrections is FBAL.	Within 0.5 s	STOP
Tr balance ABC2	1	1	1	1	1	0	1	1	The average tracking error value without the tracking servo is used as a balancing value to make corrections. The output pin for corrections is TBAL.	Within 1 s	STOP
Fo rough gain AGC1	1	1	1	1	1	1	0	0	Focus search is performed at approx. 5.4 Hz or 1.3 Hz, and the disturbance input amount for the fine AGC is determined by using focus error S-curve [P-P] value. The gain will be unchanged.	Set between 190 ms and 780 ms	FWD/ REV enabled
Tr rough gain AGC2	1	1	1	1	1	1	0	1	The [P-P] value of the tracking error in the tracking servo off status determines the disturbance input amount for the fine AGC. The gain will be unchanged.	Set between 135 ms and 350 ms	STOP
Fo fine gain FAGC	1	1	1	1	1	1	1	0	Inputs the disturbance into the focus servo loop, and adjusts the gain crossover to the frequency set by the microcomputer command.	Within 0.5 s	STOP
Tr fine gain TAGC	1	1	1	1	1	1	1	1	Inputs the disturbance into the tracking servo loop, and adjusts the gain crossover to the frequency set by the microcomputer command.	Within 0.5 s	STOP

Note) If focus balance adjustment is stopped due to automatic adjustment stoppage or focus failure, only the next focus pull-in operation will be delayed.
In order to prevent this phenomenon from occurring, it is necessary to write "0" to D2 of the SD (19F2h) after focus balance adjustment (i.e., after checking that the SENSE is set to low level).
For SD settings, refer to page 38.

7-2. I/O timing

7-2 (1) Serial data output

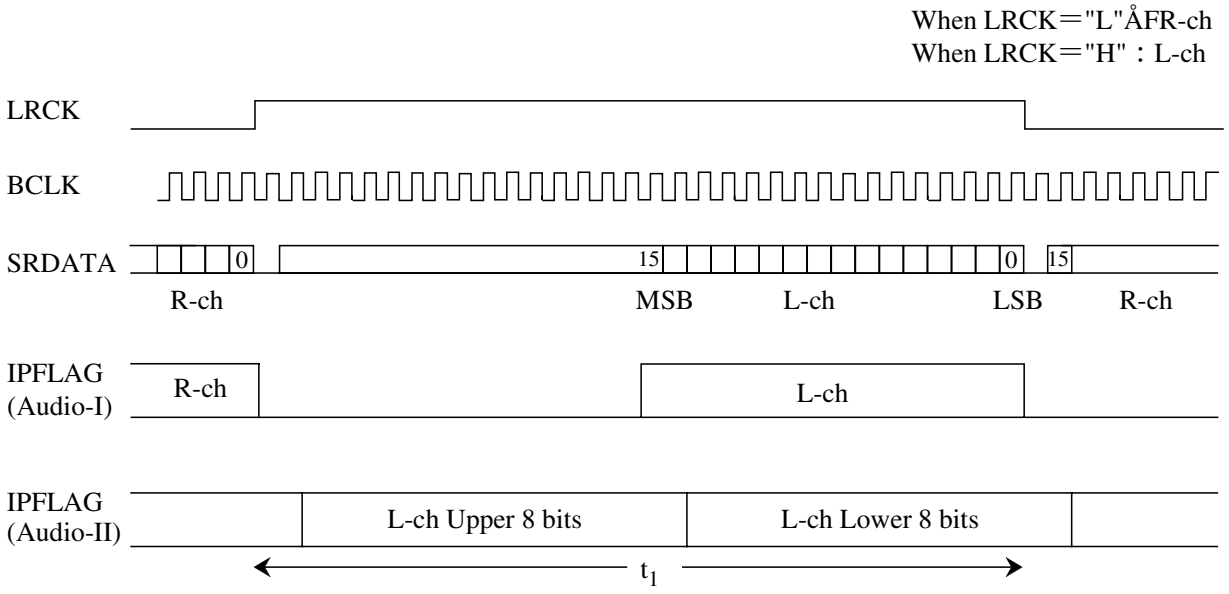


Figure 7-2-1 LRCK, BCLK, SRDATA and IPFLAG output timing

The value of t_1 is 11.34 µs at normal-speed, 5.67 µs at 2x-speed and 11.34 µs × (100 + shift amount)÷100 when the pitch controller is used.

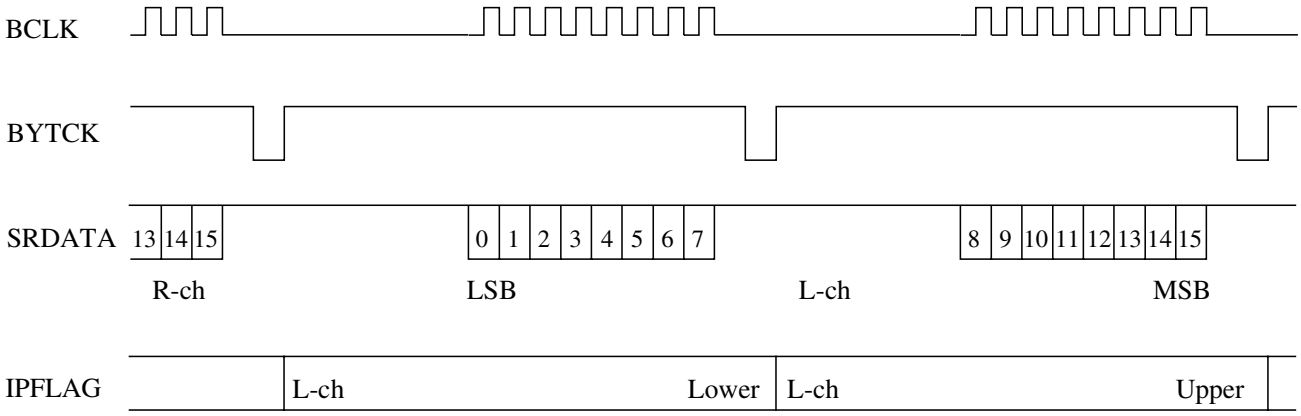


Figure 7-2-2 Output timing in CD-ROM mode

7-2 (2) Serial data output with de-emphasis function ON

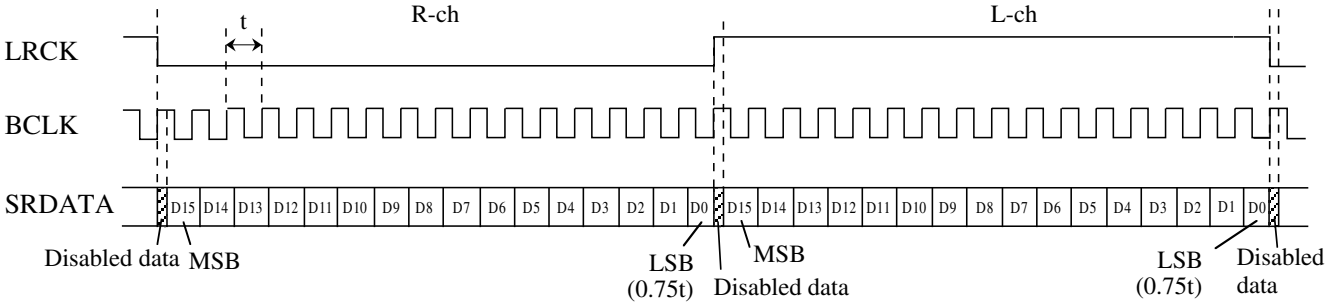


Figure 7-2-3 LRCK, BCLK and SRDATA output timing with de-emphasis function ON

The SRDATA signal is output at 32 f_S and the LSB data after each LRCK change includes 0.25t disabled data. The phase relation with the IPFLAG is not guaranteed.

7-2 (3) Serial data input format

The input data for the DF + DAC section can be given from the outside by setting the IOSEL pin to the L level. When this is done, give an LRCK input through the MSEL pin, BCLK input through the SSEL pin and SRDATA input through the PSEL pin. At this time, the internal settings of the conventional MSEL, SSEL and PSEL pins will be MSEL = L, SSEL = H and PSEL = L, respectively.

- The LRCK input frequency is fixed at 44.1 kHz. When the 2x-speed mode or jitter-free is used, a serial data input is not available in other than the DF/DAC clock fixed mode, because the performance of a D/A converter audio output is not assured. (See Table 7-1-38.)
- The BCLK input can be arbitrarily set between 16 and 32 clocks per half an LRCK cycle. However, LRCK should be changed synchronously with the falling edge of BCLK.
- The SRDATA input is an MSB-first, 2's complement type input. It should be changed synchronously with the falling edge of BCLK. Also, check that the contents of the SRDATA are L-ch data when LRCK is at the H level.
  As described above, the number of BCLK clocks can be 17 or more for each sampled data. If this is the case, the contents of the SRDATA should be back-aligned with respect to an LRCK change point, and LRCK must change before the rising edge of the next BCLK signal, after sampling the LSB of the SRDATA at the rising edge of BCLK.
- D/A converter output muting, D/A converter output polarity switching, emphasis control and peak detection DF output mode can be applied to a serial data input from an external source.
  Bilingual switching only works on a serial data output, not on a serial data input.

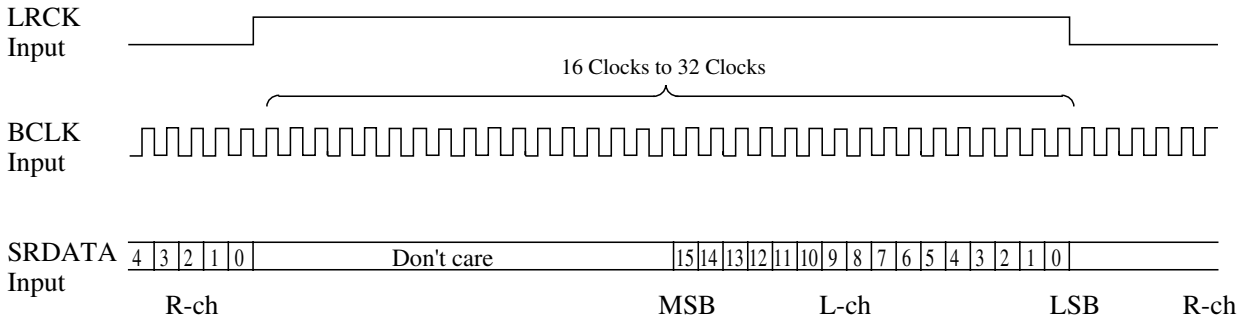


Figure 7-2-4 LRCK input (MSEL), BCLK input (SSEL) and SRDATA input (PSEL) timing when IOSEL＝L

7-2 (4) Subcode interface

A. Read SUBQ data

You can read subcode data in two ways according to the setting of the SSEL pin. The timing is shown in Figure 7-2-5.

When SSEL=L:

When SSEL pin is at L level, this LSI and the microcomputer serve as master and slave, respectively, to read SUBQ data. BLKCK and CLDCK are output at fixed frequencies of 75 Hz and 7.35 kHz, respectively. SUBQ output varies in synchronization with the falling edge of CLDCK output.

The microcomputer receives SUBQ output at the timing of the rising edge of CLDCK output. If the CRC output is OK, it is processed as correct data. The result of CRC check can be read by CRC or STAT pin.

The content of SUBQ is output as follows: S0 and S1 signals are output in synchronization with BLKCK output. Then, 80-bit subcode data are output. Then 8-bit peak detection data on the left or right channel is output twice continuously. When SSEL=L, SUBQ output is inverse one.

When SSEL=H:

When SSEL pin is at H level, this LSI and the microcomputer serve as slave and master, respectively, to read SUBQ data. The LSI receives an output signal from the microcomputer regardless of CLDCK output, and changes SUBQ output. Then, by entering 96 clocks of SQCK, all SUBQ output can be read.

The microcomputer starts the interrupt operation at the rising edge of BLKCK output. First, it checks the result of CRC of SUBQ output. If it is OK, SQCK is input to read SUBQ data.

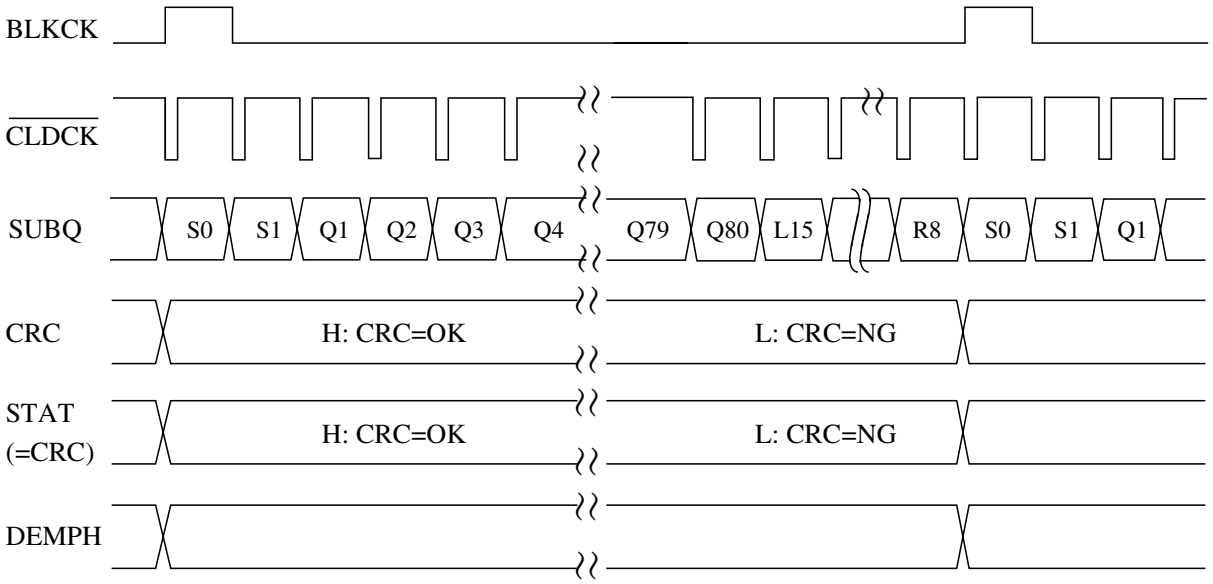
The contents of SUBQ are synchronized with the rising edge of BLKCK. First, a CRC result is output, and then, 80-bit subcode data are output every falling edge of SQCK. Then 8-bit peak detection data on the left or right channel is output twice continuously. At SSEL = H, SUBQ output is positive one.

By inputting the microcomputer command 000847h as shown in Table 7-1-4 (6), subcode data in the unit of byte is output beginning with the LSB at every falling edge of SQCK.

Read subcode data from STAT with command

By inputting the microcomputer command 78H as shown in Table 7-1-4 (11), subcode data can be read from STAT pin in synchronization with the falling edge of MCLK on condition that the SSEL pin is at H level. This mode is available only immediately after issuance of the microcomputer command 78h. This mode is cancelled when other commands are issued.

When SSEL=L (SUBQ output is inverse one):



※ H and L for all data are inverted.

When SSEL=H:

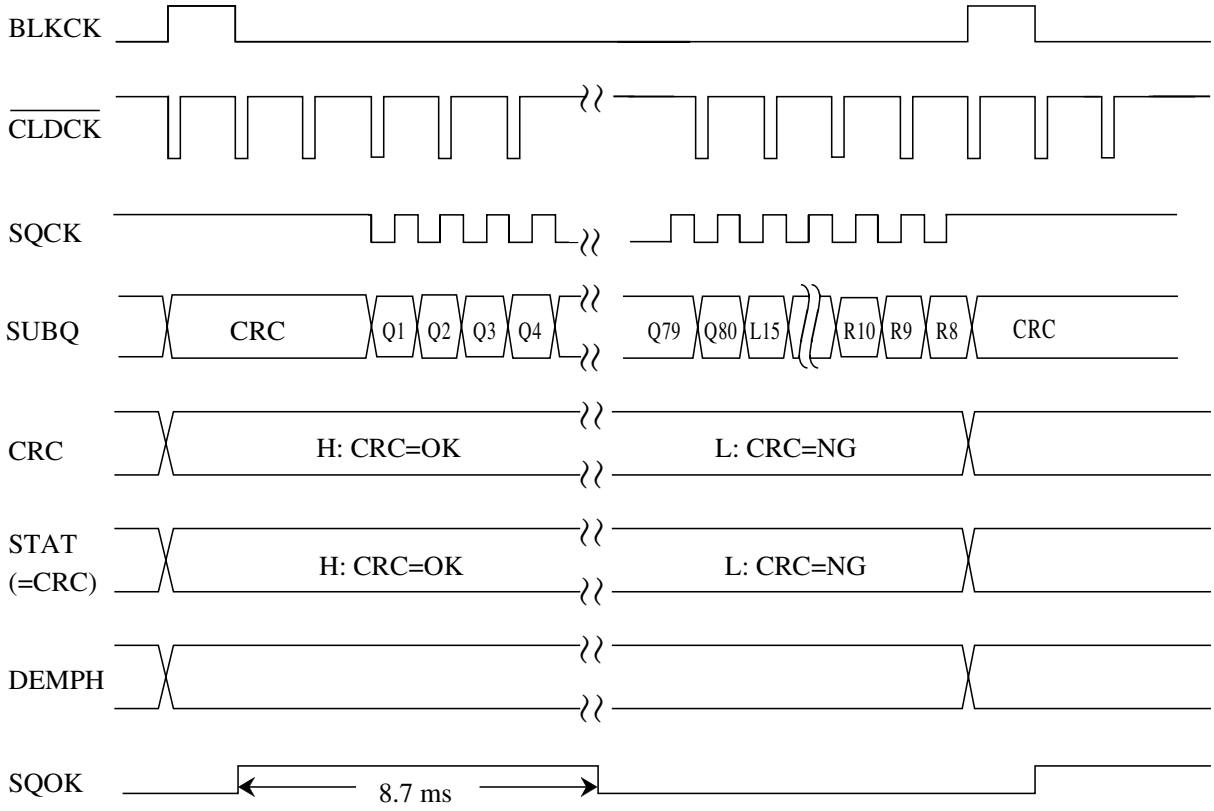
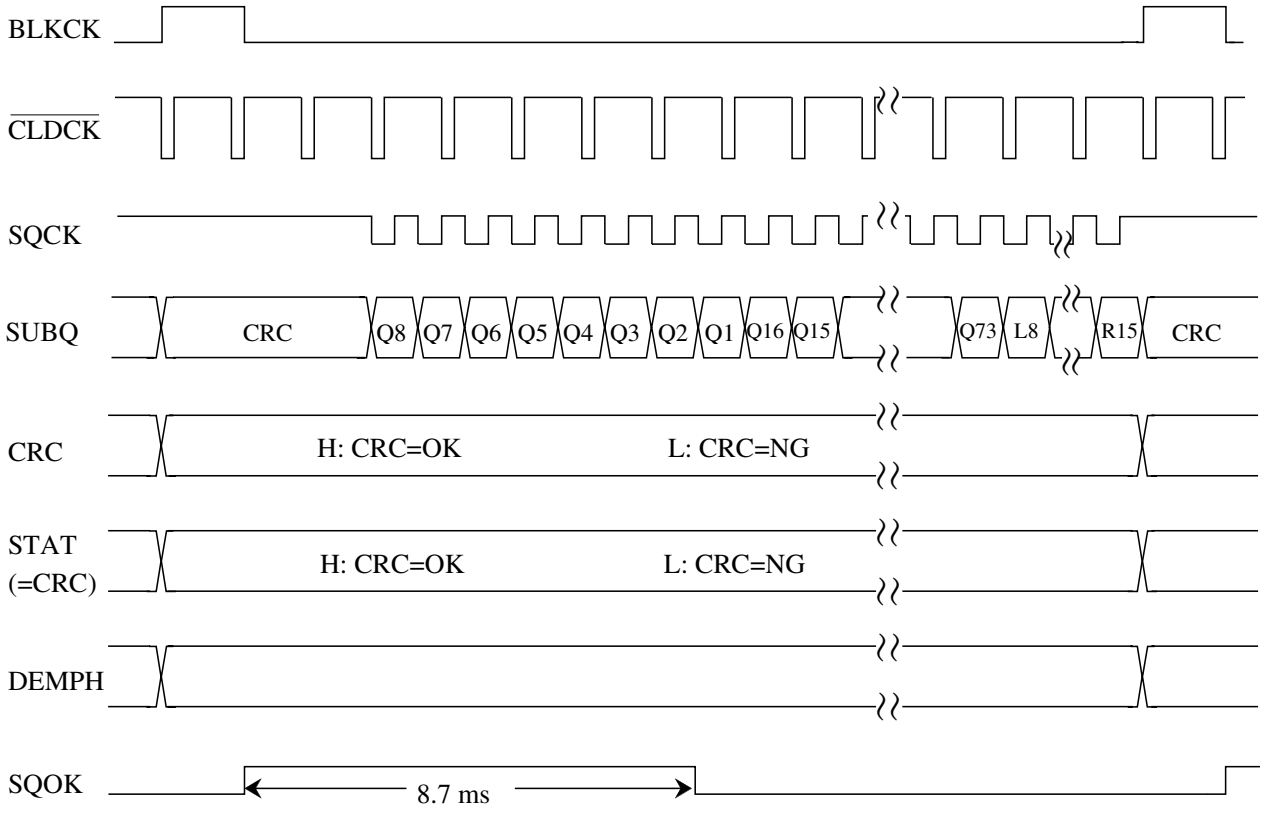


Figure 7-2-5 BLKCK, $\overline{\text{CLDCK}}$, SQCK, SUBQ, CRC and DEMPH timing

When SSEL＝H: (When microcomputer command 000847h is input)



B. Read subcode data

By inputting a clock from SBCK pin, subcode data, P to W, can be read from SUBC pin. The timing is shown in Figure 7-2-5.

Since subcode data varies every falling edge of $\overline{\text{CLDCK}}$, input 8 clocks of SBCK every falling edge of $\overline{\text{CLDCK}}$, and switch the content of SUBC output to P to W.

Then you should receive SUBC output which varies in synchronization with the falling edge of SBCK at the timing of the rising edge of SBCK. You can read all subcode data by repeating the operation above for each $\overline{\text{CLDCK}}$.

By inputting SBCK, the content of FLAG output will change. So you cannot measure the error rate when reading subcode. You must consider it in system designing.

Use of SQOK Signal

Usually the BLKCK signal is used as a trigger to start reading SUBQ data.

The data is output from the SUBQ pin in synchronization with the SQCK signal. The necessary bits of data (i.e., usually 80 bits) need to be read before the next BLKCK signal output is turned on.

The SQOK signal is set to H level for approximately 8.7 ms in the first half of the BLKCK-synchronous period. There is no need to finish reading the data while the SQOK is at H level.

The SQOK signal is used for reading SUBQ data without using BLKCK interruption. The SQCK signal is monitored by software scanning and the reading of SUBQ data is started on detection of the H-level signal. At that time, the data must be read for a maximum approx. 2 ms because the period until the next BLKCK signal output is turned on is approx. 4.6 ms.

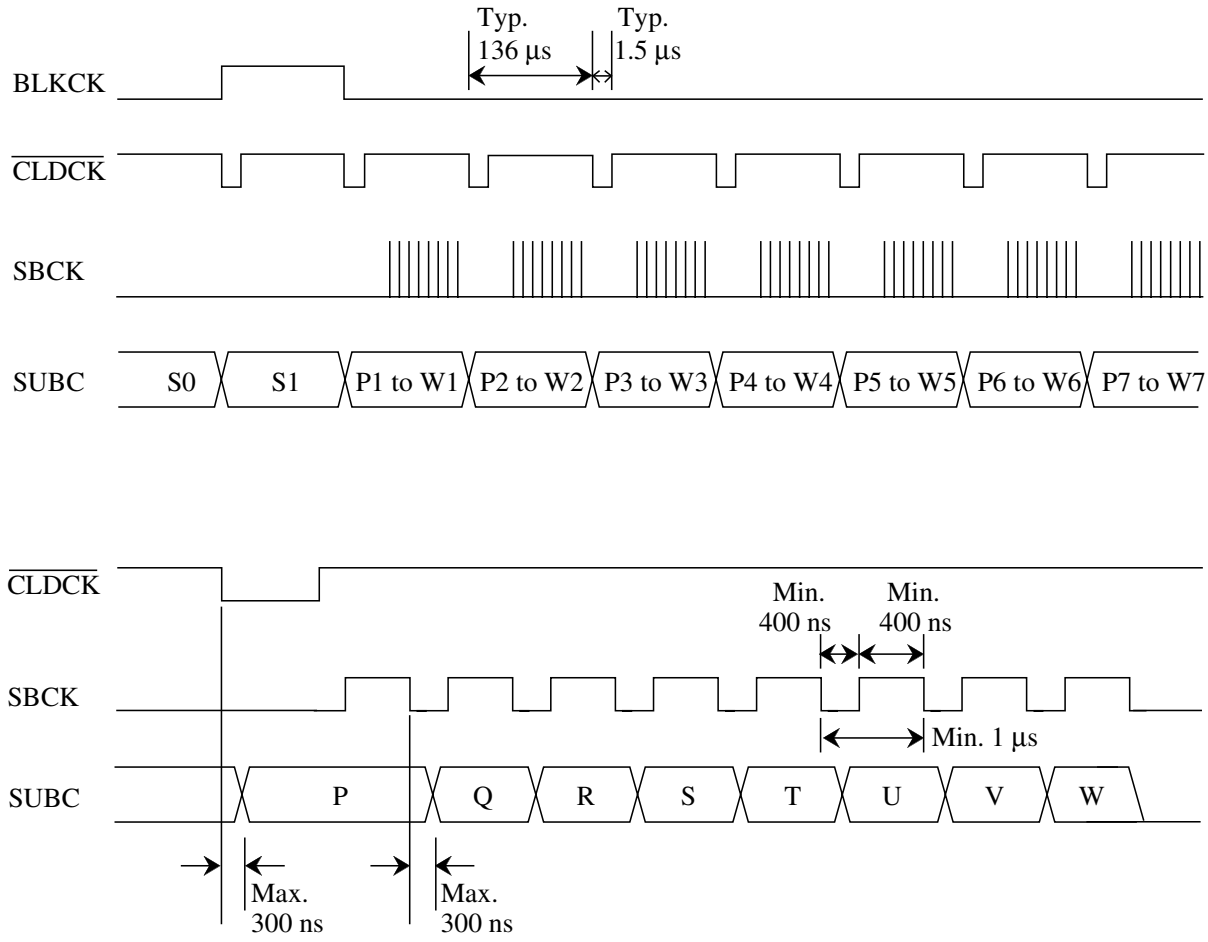


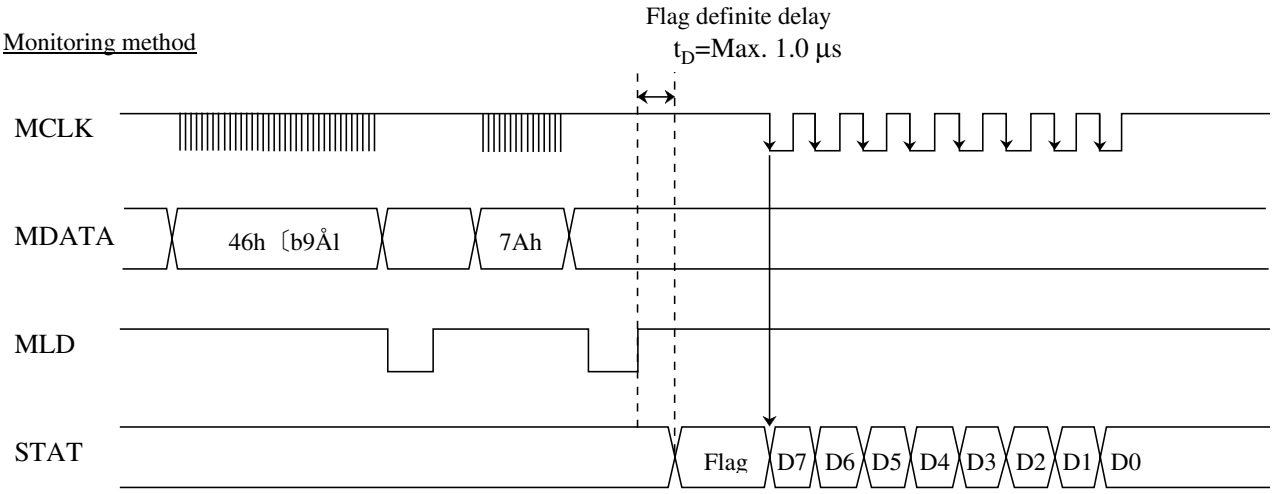
Figure 7-2-6 $\overline{\text{CLDCK}}$, SUBC and SBCK timing

7-2 (5) EDATA error rate monitor function

The error rate can be monitored through the STAT pin. The error rate is the number of frames (FLAG0=H), where C1 errors are detected, out of 2048 frames of data. The rate monitored is within an output range between 0 and 255.

By changing the command, the number of interpolation flag (IPFLAG) signals out of 2048 frames of data is monitored within an output range between 0 and 255.

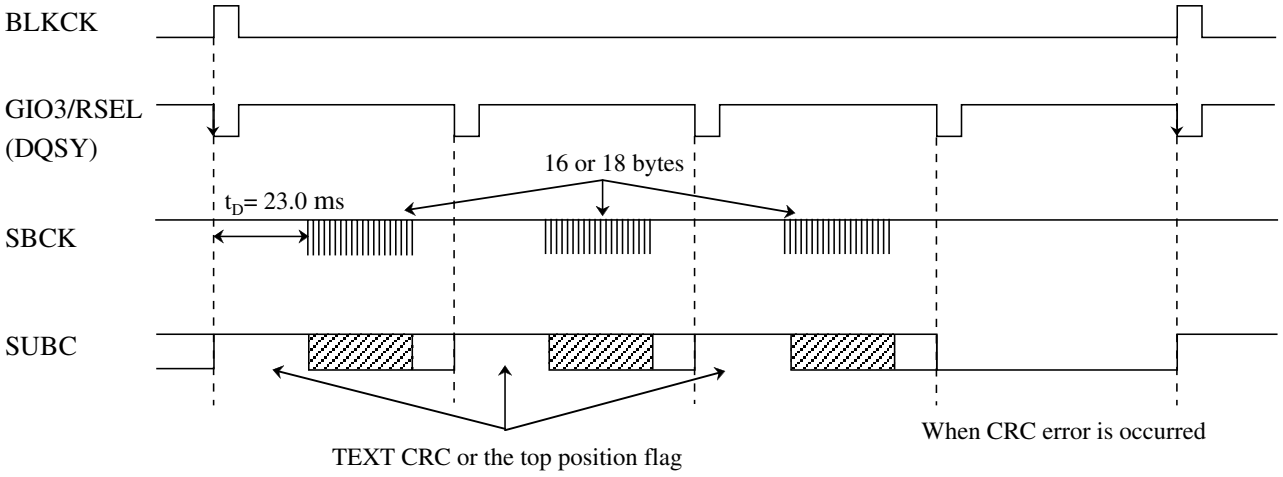
Monitoring method



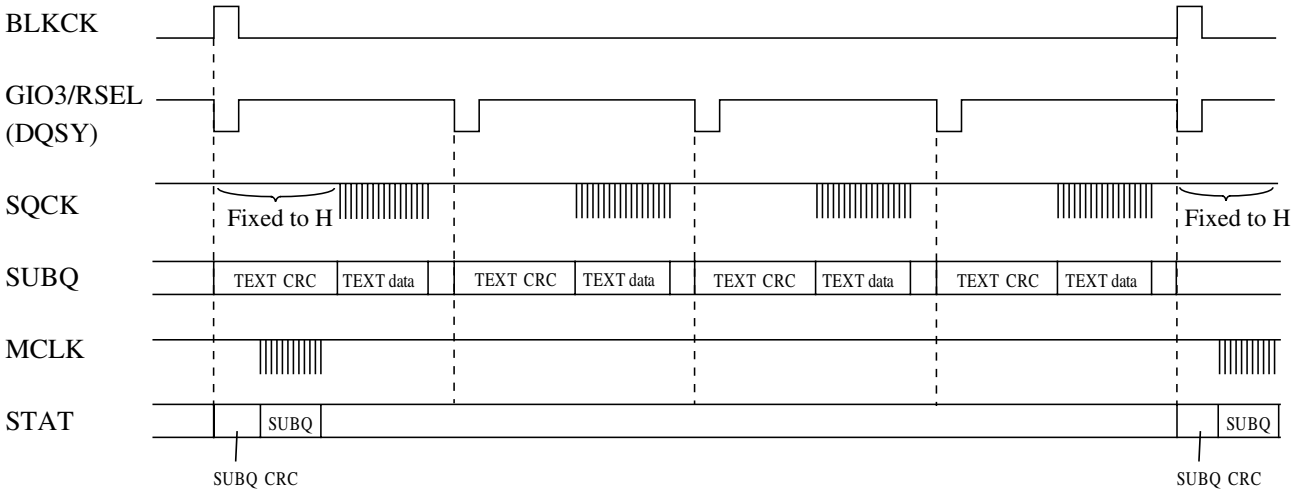
The EDATA output command 7Ah is input after setting the EDATA change command in 46h(b9).
The flag must be checked after the point of the flag definite delay.
If the flag is set to L level, there is no need to read the error rate data because the rate is the same as the error rate data previously read.
Input the MCLK signal and read the error rate if the flag is set to H level.

7-2 (6) CD-TEXT interface

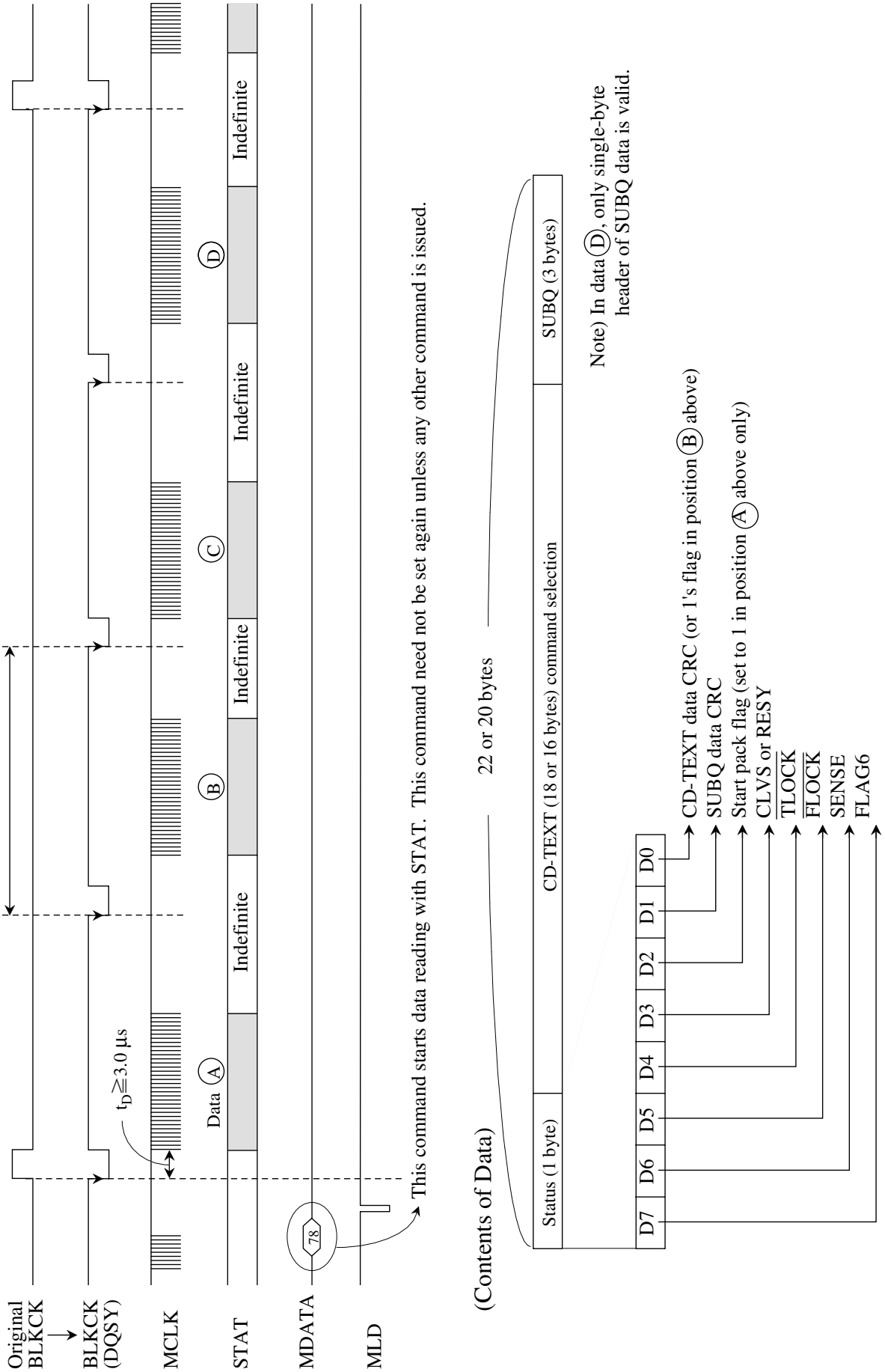
CD-TEXT mode 1



CD-TEXT mode 2



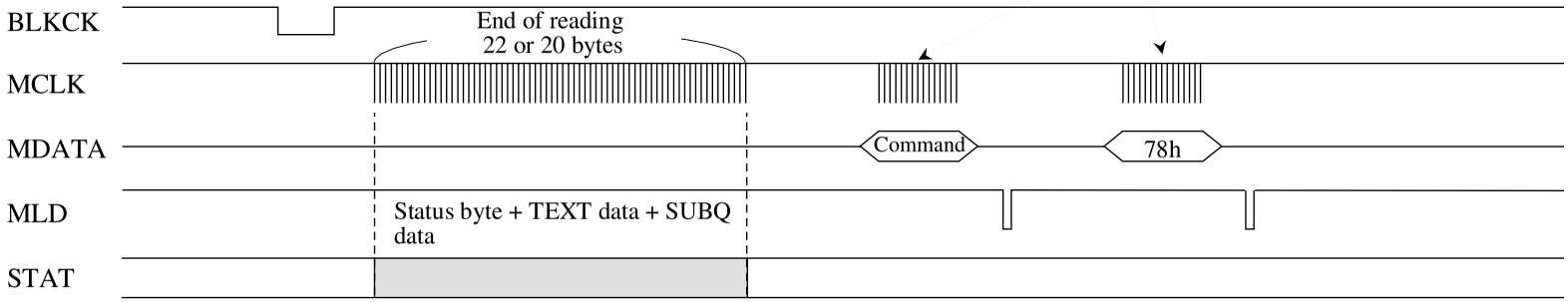
CD-TEXT M Mode 3 Fix the SQCK pin to high level when the CD-TEXT mode 3 is used.



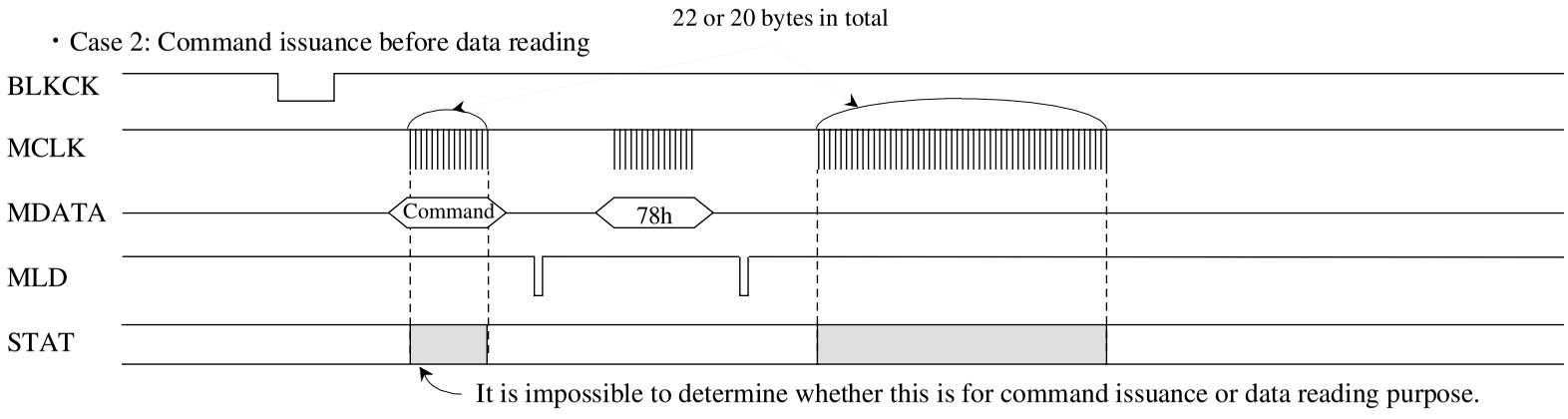
(Mode 3 Command Issuance)

The command needs to be set again if commands other than 78h are issued because such commands clear the TEXT and SUBQ data settings of STAT pin.

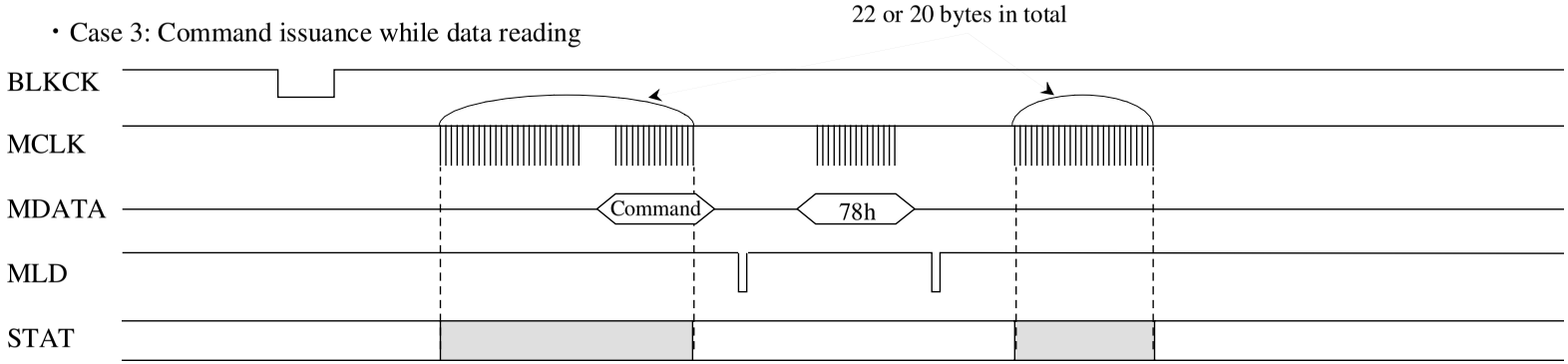
・Case 1: Command issuance at the end of data reading



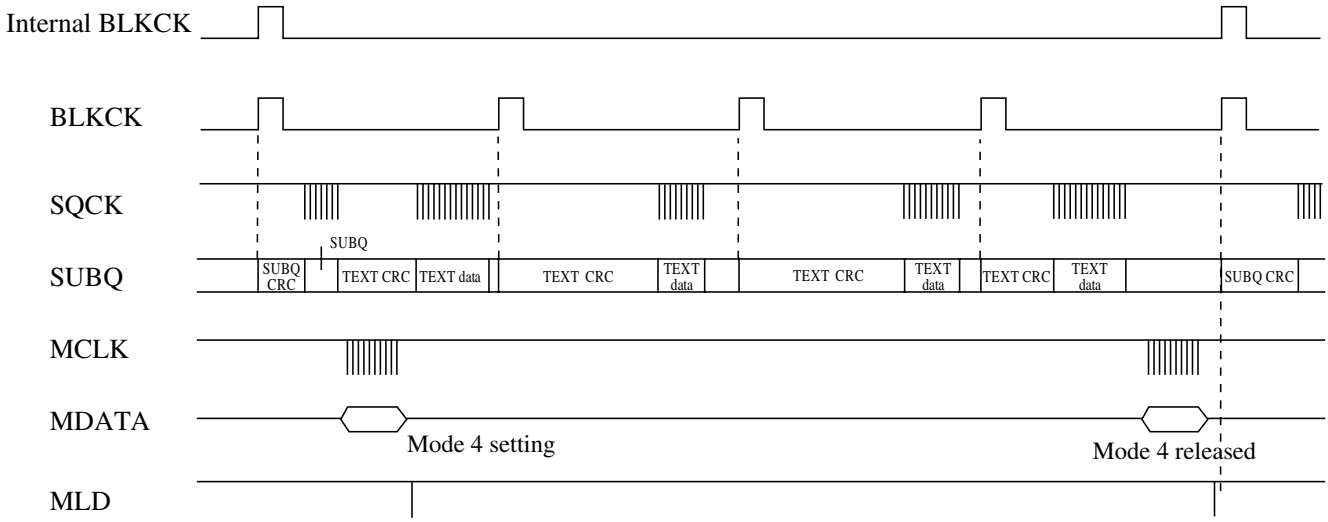
・Case 2: Command issuance before data reading



・Case 3: Command issuance while data reading



CD-TEXT Mode 4



Mode 4 must be released before the rising edge of BLKCK.

7-2 (7) Digital PLL setting

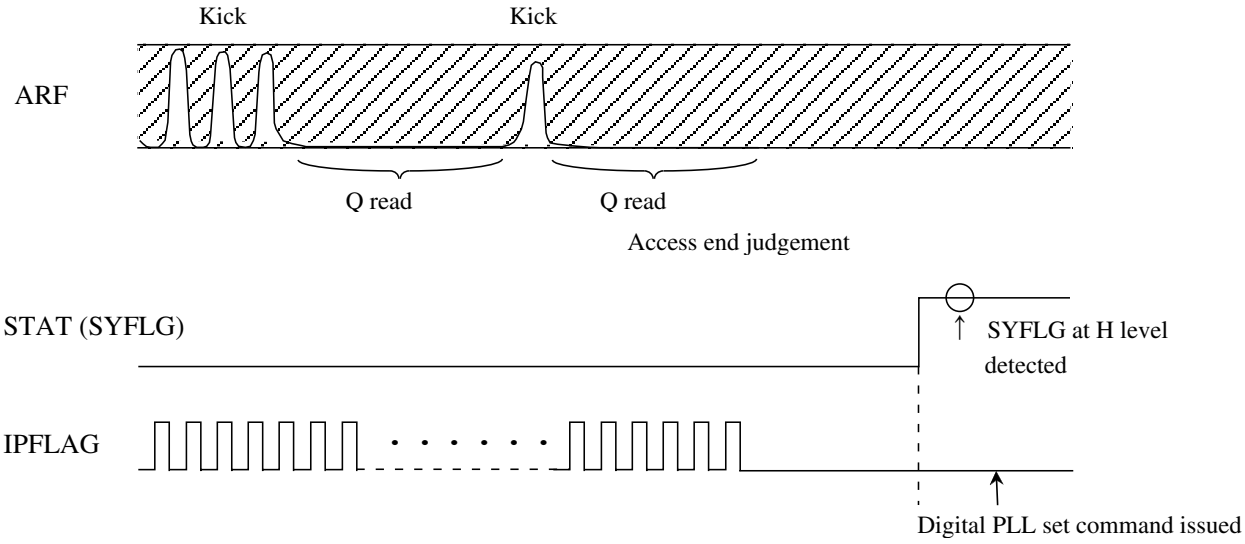
For an improvement in playability of this LSI, a digital PLL circuit is built in so that the LSI will be in stable operation without being influenced by digital noise. The lock range of this PLL circuit is not as wide as an analog PLL circuit. Therefore, a system controller is required with an analog PLL circuit employed so that the analog PLL circuit will be used in access operation and switched over to the digital PLL circuit at the end of the access operation.

The digital PLL is available in normal- and 2x-speed playback modes.

The following mode combinations can be set.

Data	Address	Function	Normal-speed playback				2x-speed playback			
D10	4E	Digital PLL operating frequency	0	×1	1	×2	1	×2	1	×2
D7		Resolution	0	1/8	1	1/16	0	1/8	1	1/16
D6		VCO oscillation frequency	0	67 MHz	0	67 MHz	0	67 MHz	1	138 MHz

Use the SYFLG (i.e., the CLV synchronous establishment detecting flag) in the following sequence to switch over the analog PLL circuit to digital PLL circuit.



Note 1) Change the digital PLL circuit over to the analog PLL circuit at the start point of the access operation. Change the digital PLL circuit over to the analog PLL circuit when the reading of the Q-code fails while the LSI is in PLAY operation. Use a sequence like the one shown above to change the digital PLL circuit over to the analog PLL circuit.

Note 2) The SYFLG can be used in playback mode after a short track jump, such as a single-track jump, or a kick. In that case, make sure that the Q-code is read properly in a sequence like the one shown above after the track jump or kick is performed.

7-2 (8) Video CD setting

It is desirable to increase the probability of correction rather than decrease the probability of error correction for video CD in playback mode. Therefore, set the C2 correction to quadruple correction.

Set the C2 correction to triple correction when playing back an audio CD.

Data	Address	Function	Video CD		Audio CD	
D6	46	Selection of C2 correction	1	Quadruple correction	0	Triple correction
D2			1		0	
D1			1		0	

7-2 (9) Digital audio interface Bit V control

D7 and D5 of microcomputer command address 42h are used for the Bit V control of the digital audio interface.

Data (16 bits)	Address (8 bits)	Function (*: Setting at reset)
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	42h	TX Bit V change (in interpolation mode)
X X X X X X X X X X 0 X X X X X		* Bit V ON
X X X X X X X X X X 1 X X X X X		Bit V OFF
		TX Bit V change (in ATT mode)
X X X X X X X X 0 X X X X X X X		* Bit V ON
X X X X X X X X 1 X X X X X X X		Bit V OFF

Note 1) The LSI in ATT mode means that the LSI is in digital attenuation, soft attenuation, or soft muting mode.
The Bit V is, however, always off if the LSI is under −12 dB control for serial data attenuation with D4 of 46h set to on.
If the Bit V is set to off in ATT mode for a TX Bit V change, the Bit V is on when the digital or soft attenuation level is set to 0 (i.e., −∞ dB).

Note 2) The Bit V is always on in TX mute control or mute control through the DMUTE pin.

7-2 (10) Audio output MUTE

The microcomuputer command makes it possible to mute SRDATA output, DF/DAC output, or TX output independently.

All outputs can be muted through the DMUTE pin.

DMUTE pin	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	Address	SRDATA output	DF/DAC output	TX output
L	X X X X X 0 X X X X X X X X X X	46	MUTE OFF	MUTE OFF	MUTE OFF
	X X X X X 1 X X X X X X X X X X		MUTE ON	MUTE OFF	MUTE OFF
	X X X X X X X X X 0 X 0 X X X X	42	MUTE OFF	MUTE OFF	MUTE OFF
	X X X X X X X X X 0 X 1 X X X X		MUTE OFF	MUTE OFF	MUTE ON
	X X X X X X X X X 1 X 0 X X X X		MUTE OFF	MUTE ON	MUTE OFF
H	X X X X X X X X X X X X X X X X	XX	MUTE ON	MUTE ON	MUTE ON

7-2 (11) Error correction

This LSI performs double correction for the C1 decoder and triple correction/quadruple correction for the C2 decoder.

- For the C2 decoder, when the data is judged impossible to correct or not highly reliable (having a high probability of erroneous correction or overlooking), it is interpolated by the interpolation circuit. (In the case of audio mode I)
- For the C1 and C2 decoders, correction results are output from the FLAG pin as FLAG0 to FLAG5.

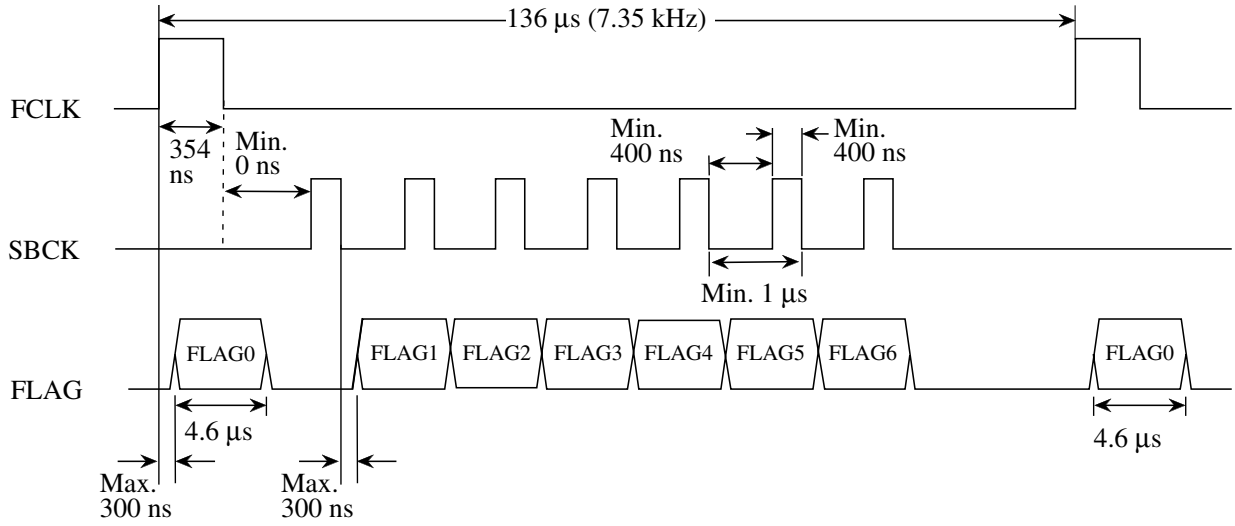
When the C1 decoder detects an error for FLAG0, "H" is output for approx. 4.6 µs, starting from the rising edge of FCLK.

FLAG1 to FLAG6 are output from FLAG pin in synchronization with the falling edge of SBCK input from the outside.

<Meanings of FLAGs>

FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	FLAG0	
×	×	×	0	0	0	C1 no error
×	×	×	0	1	1	C1 single error correction
×	×	×	1	0	1	C1 double error correction
×	×	×	1	1	1	C1 correction impossible
0	0	0	×	×	×	C2 no error
0	0	1	×	×	×	C2 single error correction
0	1	0	×	×	×	C2 double error correction
0	1	1	×	×	×	C2 double correction impossible
1	0	0	×	×	×	C2 triple error correction
1	0	1	×	×	×	C2 triple correction impossible
1	1	0	×	×	×	C2 quadruple error correction
1	1	1	×	×	×	C2 quadruple correction impossible

Flag Output Timings (At Normal-Speed)



※ If the falling edge of clock is input to SBCK while FLAG0 is being output, an output from FLAG pin will be switched from FLAG0 to FLAG1.

PRODUCT STANDARDS

A. ABSOLUTE MAXIMUM RATINGS

T_a = 25 ℃

Parameter		Symbol	Rating	Unit	Note
A1	Supply voltage	V_{DD} AV_{DD}	−0.3 to +4.6	V	V_{SS}=0 V AV_{SS}=0 V
A2	5-V reference voltage	V_{CC5V}	−0.3 to +5.7	V	V_{SS}=0 V AV_{SS}=0 V
A3	Input voltage	V_I	V_{SS}−0.3 to V_{DD}+0.3 AV_{SS}−0.3 to AV_{DD}+0.3	V	V_{SS}=0 V AV_{SS}=0 V
A4	Output voltage	V_O	V_{SS}−0.3 to V_{DD}+0.3 AV_{SS}−0.3 to AV_{DD}+0.3	V	V_{SS}=0 V AV_{SS}=0 V
A5	Power dissipation	P_D	580	mW	V_{SS}=0 V AV_{SS}=0 V T_a = 85 ℃ (Note 7)
A6	Operating ambient temperature	T_{opr}	−30 to +85	℃	
A7	Storage temperature	T_{stg}	−55 to +125	℃	

Note 1) The absolute maximum ratings are the limit values beyond which the device may be broken. They do not assure operations.

Note 2) Each of V_{SS}, DV_{SS1}, AV_{SS1} and AV_{SS2} pins should be directly connected to the ground and used at the same voltage.

Note 3) Each of V_{DD}, DV_{DD1}, AV_{DD1} and AV_{DD2} pins should be directly connected to the specified power supply and used at the same voltage.

Note 4) V_{DD}, DV_{DD1}, AV_{DD1} and AV_{DD2} should be powered up at the same time.

Note 5) Connect a bypass capacitor (0.1 µF or more) between V_{DD} and V_{SS} pins, between DV_{DD1} and DV_{SS1} pins, between AV_{DD1} and AV_{SS1} pins, between AV_{DD2} and AV_{SS2} pins and between V_{REF} and V_{SS} pins.

Note 6) The operation of the audio D/A converter is guaranteed only for operation in normal-speed playback mode.

Note 7) Condition: This LSI shall be mounted on a standard glass epoxy board (75 mm×75 mm×0.8 mm).

B. OPERATING CONDITIONS

T_a = −30 ℃ to +85 ℃, V_{SS} = 0 V
AV_{SS} = 0 V

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
B1	Digital system supply voltage	V_{DD}	Normal-and 2x-speed playback modes	3.0	3.3	3.6	V
B2	Analog system supply voltage	AV_{DD}	Normal-and 2x-speed playback modes	3.0	3.3	3.6	V
B3	Digital system supply voltage	V_{DD1}	4x-speed playback mode	3.2	3.3	3.6	V
B4	Analog system supply voltage	AV_{DD1}	4x-speed playback mode	3.2	3.3	3.6	V
B5	5-V reference voltage	V_{CC5V}		4.75	5.0	5.25	V

Note 9) It is recommended to basically use AV_{DD} at the same voltage as DV_{DD}.

T_a = −30 ℃ to +85 ℃, V_{SS} = 0 V
V_{DD} = 3.3 V, AV_{SS} = 0 V

Self-excited Oscillation 1 (Note 10)

B6	Crystal frequency	f_{xtal}	CSEL = L		16.9344		MHz
B7	External capacitance 1	C1			5		pF
B8	External capacitance 2	C2			5		pF

External Clock Input 1 (Note 11), (Note 12)

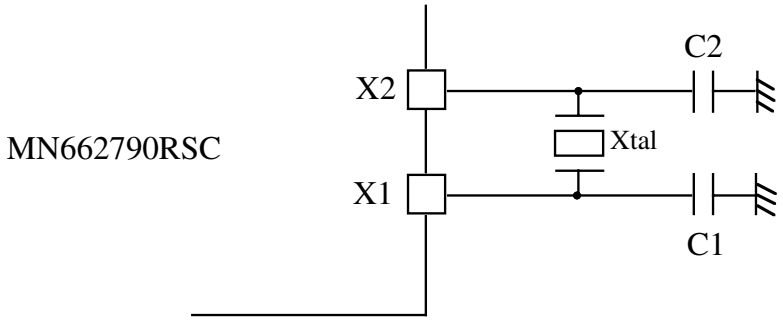
B9	Clock input frequency	f_{X1}	CSEL = L C3 = 1000 pF Switching level V_{X1}/2		16.9344		MHz
B10	Clock input amplitude	V_{X1}		2.0			V[P-P]
B11	High-level pulse width	t_{X1H}		26	29.5		ns
B12	Low-level pulse width	t_{X1L}		26	29.5		ns
B13	External capacitance 3	C3		1000			pF

External Clock Input 2 (Note 11), (Note 12)

B14	Clock input frequency	f_{X1}	CSEL = H C3 = 1000 pF Switching level V_{X1}/2		33.8688		MHz
B15	Clock input amplitude	V_{X1}		2.0			V[P-P]
B16	High-level pulse width	t_{X1H}		13	14.8		ns
B17	Low-level pulse width	t_{X1L}		13	14.8		ns
B18	External capacitance 3	C3		1000			pF

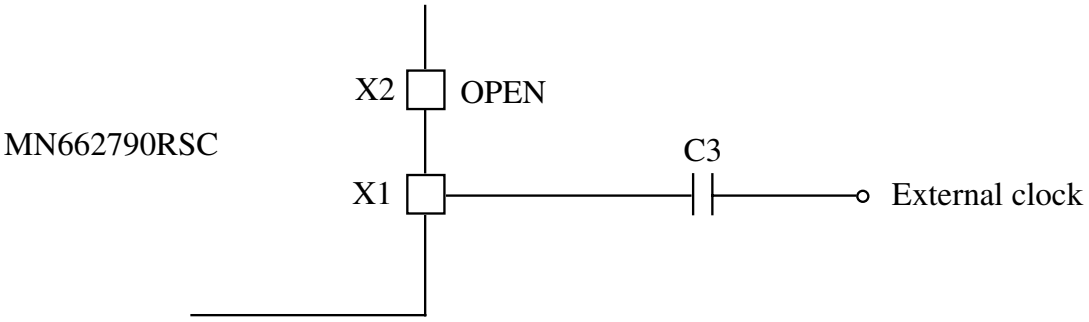
T_a = −30 ℃ to +85 ℃, V_{SS} = 0 V
V_{DD} = 3.3 V, AV_{SS} = 0 V

Note 10) Oscillation circuit

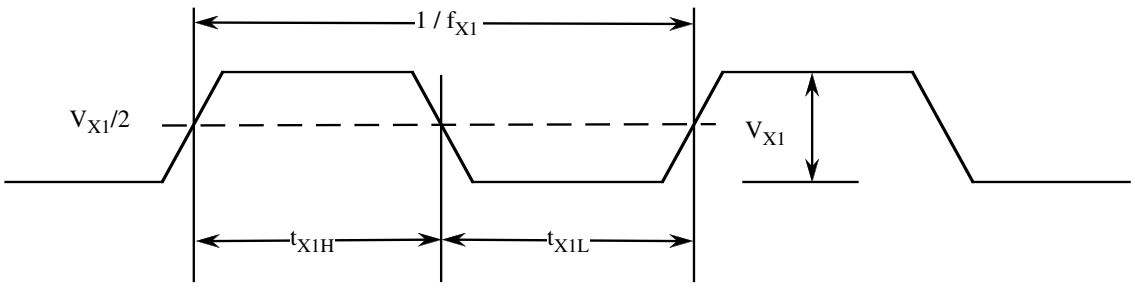


The appropriate capacitors' values differ according to the oscillator used. Use the values specified by the oscillator manufacturer.

Note 11) External clock input 1



Note 12) External clock



C. Electrical Characteristics

(1) DC Characteristics

V_{CC5V} = 5.0 V
V_{SS} = 0 V
$AV_{DD} = V_{DD}$, AV_{SS} = 0 V
T_a = −30 ℃ to +85 ℃
f_{X1} = 16.9344 MHz

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
C1	Supply current	I_{DD}	V_{DD}=3.3 V No external load during normal-speed playback mode T_a=25 ℃ f_{X1}=16.9344 MHz CSEL=L		45	100	mA
C2	Total power consumption	P_{tot}			150	330	mW
C3	Supply current	I_{DD}	V_{DD}=3.3 V No external load during 2x-speed playback mode T_a=25 ℃ f_{X1}=16.9344 MHz CSEL=L When DF/DAC clock fixed mode is set.		50	103	mA
C4	Total power consumption	P_{tot}			170	340	mW
C5	Supply current	I_{DD}	V_{DD}=3.3 V No external load during 4x-speed playback mode T_a=25 ℃ f_{X1}=16.9344 MHz CSEL=L When DF/DAC clock fixed mode is set.		60	105	mA
C6	Total power consumption	P_{tot}			200	345	mW

V_{CC5V}＝5.0 V
V_{DD}＝3.3 V, V_{SS}＝0 V
AV_{DD}＝3.3 V, AV_{SS}＝0 V
T_a＝－30 ℃ to ＋85 ℃
f_{X1}＝16.9344 MHz or 33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	Input Pins (1) ＊1						
C7	Input voltage high level	V_{IH1}		$0.7V_{DD}$		V_{DD}	V
C8	Input voltage low level	V_{IL1}		0		$0.3V_{DD}$	V
C9	Input leakage current	I_{LK1}	V_{IN}＝0 to V_{DD}			±1	μA
	Input Pins (2) ＊2						
C10	Input voltage high level	V_{IH2}		2.0		V_{CC5V}	V
C11	Input voltage low level	V_{IL2}		0		0.8	V
C12	Input leakage current	I_{LK2}	V_{IN}＝0 to V_{CC5V}			±1	μA
	Input Pin (3) SBCK						
C13	Input voltage high level	V_{IH3}		2.0		5.25	V
C14	Input voltage low level	V_{IL3}		0		0.8	V
C15	Input leakage current	I_{LK3}	V_{IN}＝0 V to 5.25 V			±1	μA

＊1 TEST3, OFT, $\overline{\text{RFDET}}$, BDO, $\overline{\text{TEST}}$, IOSEL
＊2 MCLK, MDATA, MLD, SQCK/GIO0, DMUTE, $\overline{\text{RST}}$, RSEL/GIO3, CSEL, PSEL, SSEL, MSEL

V_{CC5V}＝5.0 V
V_{DD}＝3.3 V, V_{SS}＝0 V
AV_{DD}＝3.3 V, AV_{SS}＝0 V
T_a＝－30 ℃ to ＋85 ℃
f_{X1}＝16.9344 MHz or 33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	Output Pins (1) ＊3						
C16	Output voltage high level	V_{OH1}	I_{OH1}＝－2.0 mA	V_{DD}－0.6			V
C17	Output voltage low level	V_{OL1}	I_{OL1}＝2.0 mA			0.4	V
	Output Pins (2) ＊4						
C18	Output voltage high level	V_{OH2}	I_{OH2}＝－2.0 mA	V_{DD}－0.6			V
C19	Output voltage low level	V_{OL2}	I_{OL2}＝2.0 mA			0.4	V
C20	Output leakage current (ECM)	I_{LK2}	Hi-Z V_o＝0 V to 3.3 V			±1	μA

＊3 BCLK, LRCK, SRDATA, SENSE, $\overline{\text{FLOCK}}$, SUBQ, STAT, SMCK, PC, LDON, WVEL, EFM, PCK, SUBC, BYTCK/TRVSTP, GIO1/$\overline{\text{CLDCK}}$, GIO2/FCLK, IPFLAG, CLVS, CRC, DEMPH, TX, BLKCK, FLAG, RESY/FLAG6

＊4 ECM

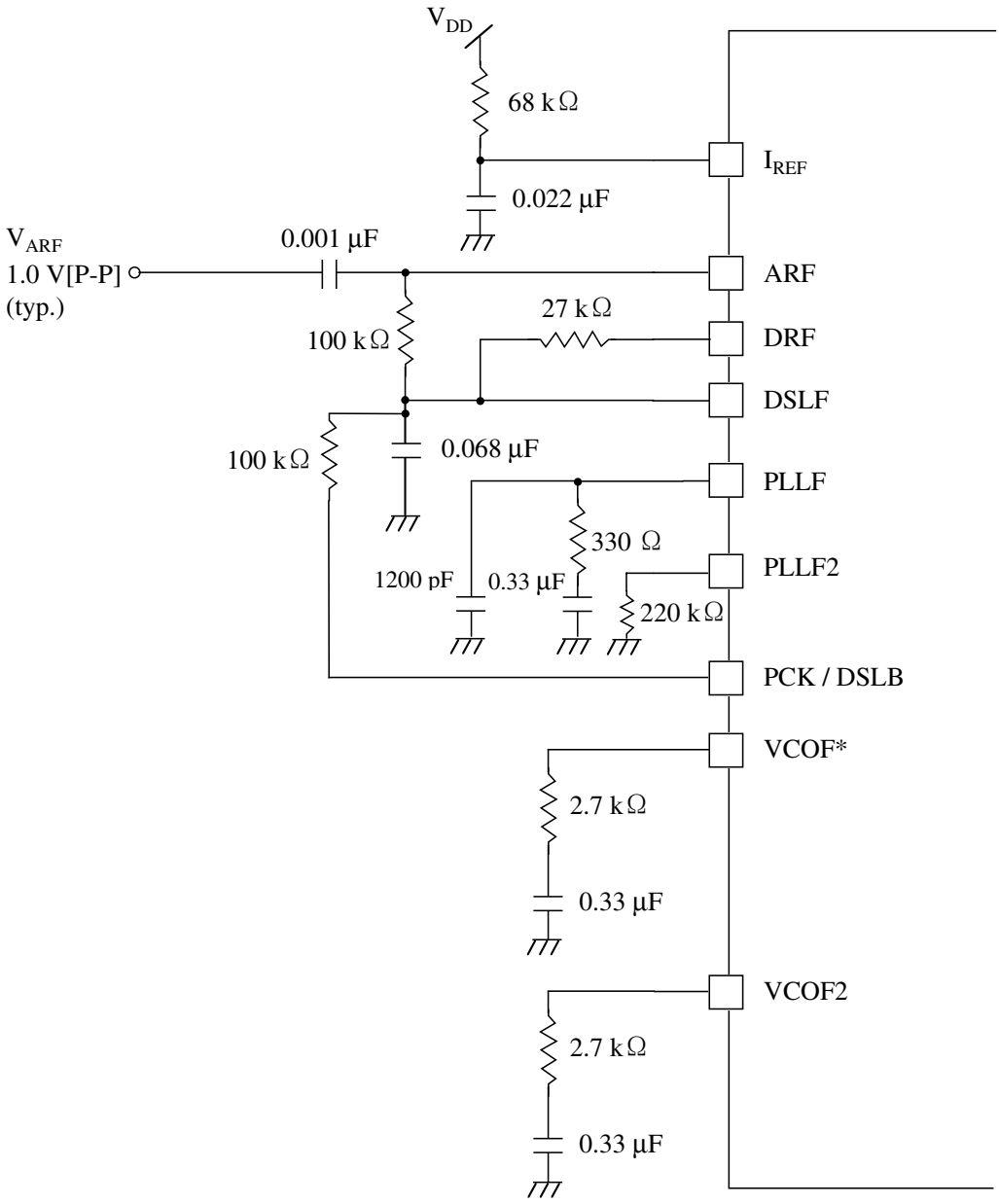
V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	Analog System Input Pin (1) I_{REF}						
C21	Input current	I_{REF}	When pulled up by a 120-kΩ resistor	11	20	28	µA
	Analog System Input Pin (2) ARF						
C22	Input signal amplitude	V_{ARF}	Input level of the EFM signal in the application circuit of the DSL circuit block	0.5	1.0		V[P-P]
C23	Input leakage current	I_{LKA}				±1	µA
	Analog System Input Pin (3) DRF						
C24	Input leakage current	I_{LKA}				±1	µA
C25	Internal resistance between ARF and DRF pins	R_{DRF}	2x-speed playback mode ARF=1.65 V			10	kΩ
	Analog System Output Pin (1) DSLF (I_{REF} pin is pulled up to AV_{DD} by a 120-kΩ resistor) (Note 13)						
C26	Output current (N)	I_{DSH}	BDO=L, Tracking ON-state DSLF=1.65 V, ARF=3.3 V	+45	+59	+75	µA
C27	Output current (P)	I_{DSL}	BDO=L, Tracking ON-s tate DSLF=1.65 V, ARF=0 V	−45	−59	−75	µA
C28	Output unbalance current	$I_{DSH}+I_{DSL}$	DSLF=1.65 V Normal current output mode	−7.0	−1.0	+5.0	µA
	Analog System Output Pin (2) PLLF (I_{REF} pin is pulled up to AV_{DD} by a 120-kΩ resistor)						
C29	Phase comparison output current (N)	I_{PFH}	BDO=L, Tracking OFF-state	52	67	89	µA
C30	Phase comparison output current (P)	I_{PFL}	BDO=L, Tracking OFF-state	−52	−67	−89	µA
C31	Phase comparison output unbalance current	$I_{PFH}+I_{PFL}$	BDO=L, Tracking OFF-state Normal current output mode	−8.55	−2.55	+4.45	µA
C32	Leakage current	I_{LKP1}	Hi-Z			±1	µA
C33	VCO oscillation frequency 1	f_{VCO1}	Normal-speed playback mode (With I_{REF} pin as shown in the recommended circuit diagram)	3.71		4.92	MHz

V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	Analog System Output Pin (2) PLLF (I_{REF} pin is pulled up to AV_{DD} by a 120-kΩ resistor)						
C34	VCO oscillation frequency 2	f_{VCO2}	2x-speed playback mode (With I_{REF} pin as shown in the recommended circuit diagram)	7.42		9.84	MHz
C35	VCO oscillation frequency 3	f_{VCO3}	4x-speed playback mode (With I_{REF} pin as shown in the recommended circuit diagram)	14.84		25.93	MHz
	Analog System Output Pin (3) VCOF (I_{REF} pin is pulled up to AV_{DD} by a 120-kΩ resistor)						
C36	Phase comparison output current (N)	I_{VFH}		40	54	71	µA
C37	Phase comparison output current (P)	I_{VFL}		−40	−54	−71	µA
C38	Input leakage current	I_{LKV}	Hi-Z			±1	µA
C39	Jitter-free VCO oscillation frequency	f_{VCO4}	With I_{REF} pin as shown in the recommended circuit diagram (4x-speed mode) With I_{REF} pin as shown in the recommended circuit diagram (2x-speed mode) With I_{REF} pin as shown in the recommended circuit diagram (Normal-speed mode)	19.6438 9.8219 4.9109	33.8688 16.9344 8.4672	50.8032 25.4016 12.7008	MHz
	Analog System Output Pin (4) PLLF2 (I_{REF} pin is pulled up to AV_{DD} by a 120-kΩ resistor)						
C40	Leakage current	I_{LKP2}				±1	µA
C41	Internal resistance between PLLF and PLLF2 pins	R_{PLLF}	PLLF=1.65 V			250	Ω
	Analog System Input Pin (4) TRCRS						
C42	Input signal amplitude	V_{TRC}	TRCRS signal input level (with V_{REF} level as a center)	2			V[P-P]
C43	Input leakage current	I_{LKT}				±1	µA
	Analog System Output Pin (5) VCOF2 (I_{REF} pin is pulled up to AV_{DD} by a 120-kΩ resistor)						
C44	Phase comparison output current (N)	I_{VFH2}		40	54	71	µA
C45	Phase comparison output current (P)	I_{VFL2}		−40	−54	−71	µA
C46	Input leakage current	I_{LKV2}	Hi-Z			±1	µA
C47	VCO oscillation frequency	f_{VCO5}	With I_{REF} pin as shown in the recommended circuit diagram		33.8688		MHz

V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz



Recommended Circuit Diagram to DSL / PLL and Jitter-free VCOF Blocks

* When 4x-speed playback mode with a 16.9344-MHz clock or a jitter-free function is not used, connect the VCOF pin to V_{DD} or ground.
* It is necessary to change a value of the resistor connected to I_{REF} pin to adjust the oscillation frequency in 4x-speed playback mode.

Note 13) Insert a 100-kΩ resistor between the DSLF and PCK / DSLB pins or between the DSLF and DSLBDA pins to use the DSL balance correction function.

Note 14) This recommended circuit is typical, so it is necessary to choose external components' values with due regard to playability.

V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	Analog System Input Pins (5) TE, FE, RFENV						
C48	Input voltage high level	V_{IH4}				AV_{DD}	V
C49	Input voltage low level	V_{IL4}		0			V
	Analog System Input Pin (6) V_{REF}						
C50	Input voltage	V_{I5}			$0.5AV_{DD}$		V
	Analog System Output Pins (6) TVD, TRD, FOD, TBAL, FBAL, ECS, DSLBDA						
C51	Load characteristic	V_{O4}	Load: ±300 µA Difference from no load state at 20 %, 50 % and 80 % of full-scale.			±4.0	LSB

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V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
A/D Converter Desired Values (for Servo)							
C52	Resolution	RES				8	bit
C53	Integral nonlinearity	INL	A/D output=80 to 7F (2's complement)			±2	LSB
C54	Differential nonlinearity	DNL				±3	LSB
D/A Converter Desired Values (for Servo)							
C55	Resolution	RES				8	bit
C56	Integral nonlinearity	INL				±2	LSB
C57	Differential nonlinearity	DNL				±0.82	LSB
C58	Offset	$DOFF_1$	Digital input 0 (2's complement) Value to 1.65-V output No load			±10	LSB
C59	Offset	$DOFF_2$	Value at 25 % of the full-scale No load			±10	LSB
C60	Offset	$DOFF_3$	Value at 75 % of the full-scale No load			±10	LSB

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T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

Parameter	Symbol	Conditions	Limits			Unit
			min	typ	max	
D/A Converter Desired Values Analog Characteristics (Note 15), (Note 18)						
C61 Signal to noise ratio	S/N	EIAJ	90	97		dB
C62 Dynamic range	D.R.	EIAJ	80	88		dB
C63 Total harmonic distortion	THD+N	EIAJ		0.007	0.013	%
C64 Crosstalk		EIAJ	70	80		dB
C65 Output level 1		f=1 kHz Full-scale output (Note 16)	1.12	1.32	1.55	Vrms
C66 Output level difference		Difference of OUTL and OUTR pins at output level 1. 20 log (V_R/V_L)	−0.99		+0.99	dB
C67 Output level 2		f=1 kHz Full-scale output (Note 17)	0.68	0.79	0.93	Vrms

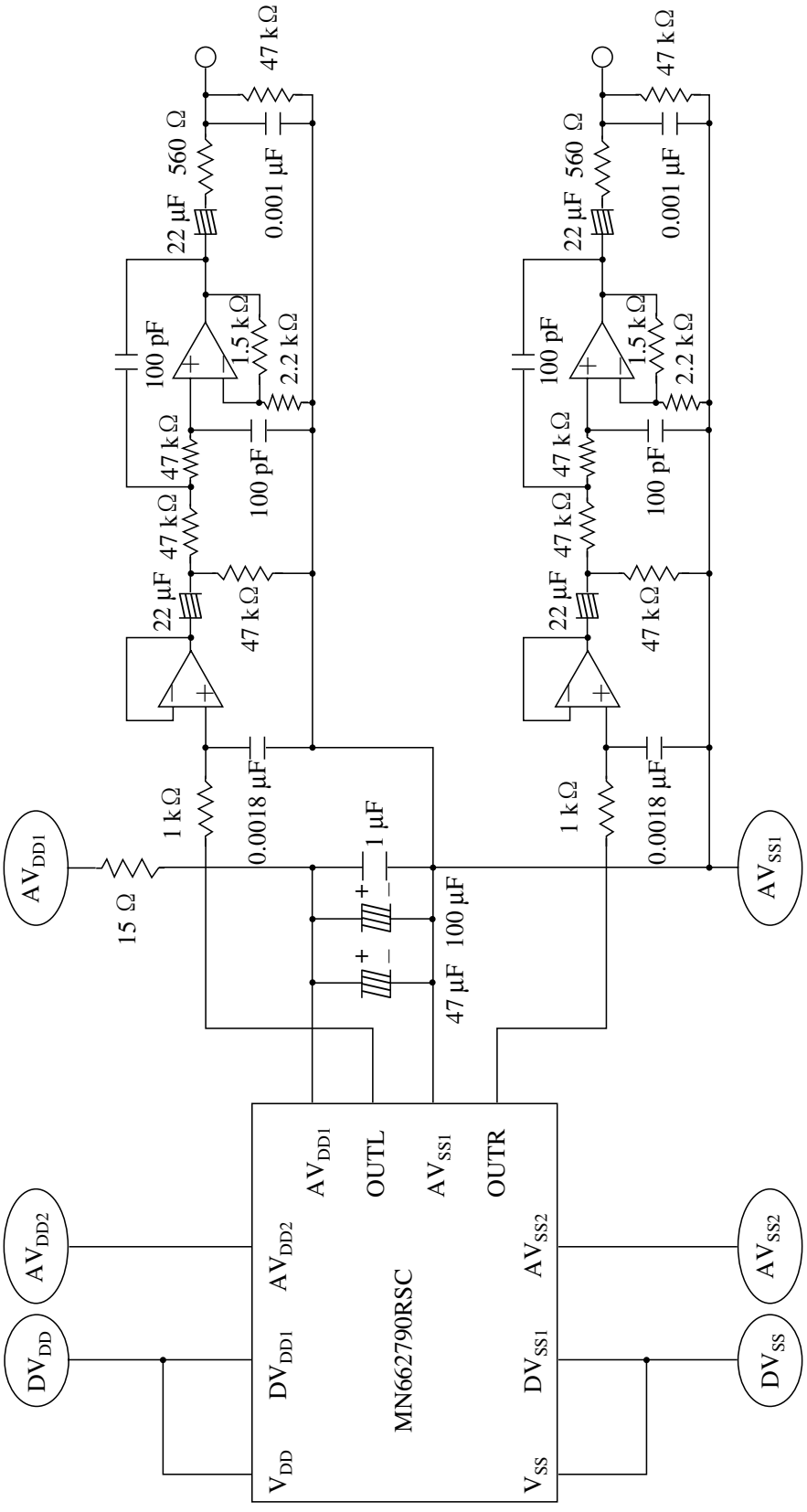
Note 15) The analog characteristics indicate the values measured by inserting a 15-Ω resistor between the AV_{DD1} pin and power supply. The typical values are only reference values. They are not guaranteed.

Note 16) The output level 1 shows the measured value at the output pins of the application circuit.

Note 17) The output level 2 shows a value at the output pin of this LSI and is calculated by taking the measured value of output level 1, dividing it by the external circuit gain of the application circuit.

Note 18) Use the D/A converter only in the normal-speed playback mode. Operation of the D/A converter cannot be guaranteed when it is used in the 2x-and 4x-speed modes.

[D/A Converter Application Circuit]



V_{CC5V}=5.0 V
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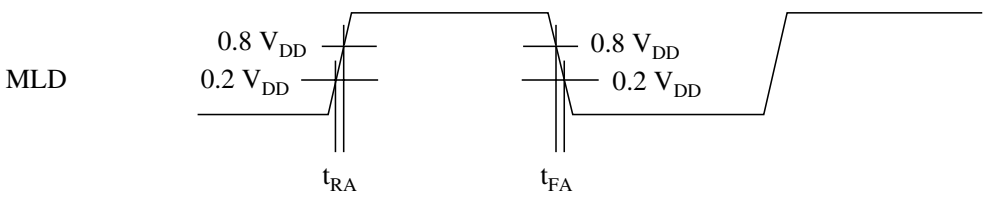
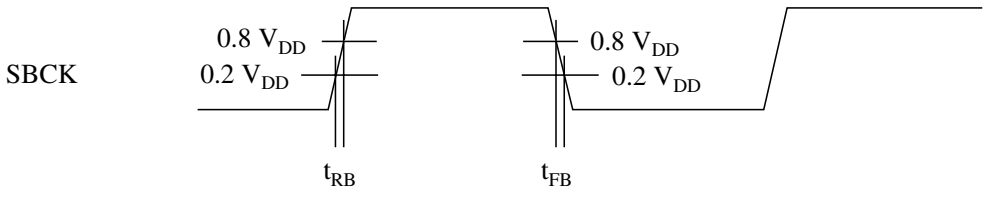
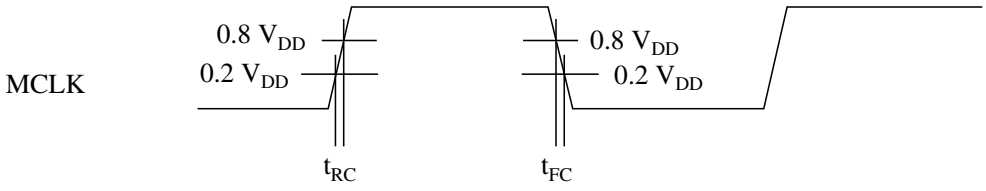
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
C68	Rise time	t_{RA}	There should be no noise greater than 20 mV[P-P] in signal lines and power supply.			250	ns
C69	Fall time	t_{FA}				250	ns
C70	Rise time	t_{RB}				100	ns
C71	Fall time	t_{FB}				100	ns
C72	Rise time	t_{RC}				100	ns
C73	Fall time	t_{FC}				100	ns

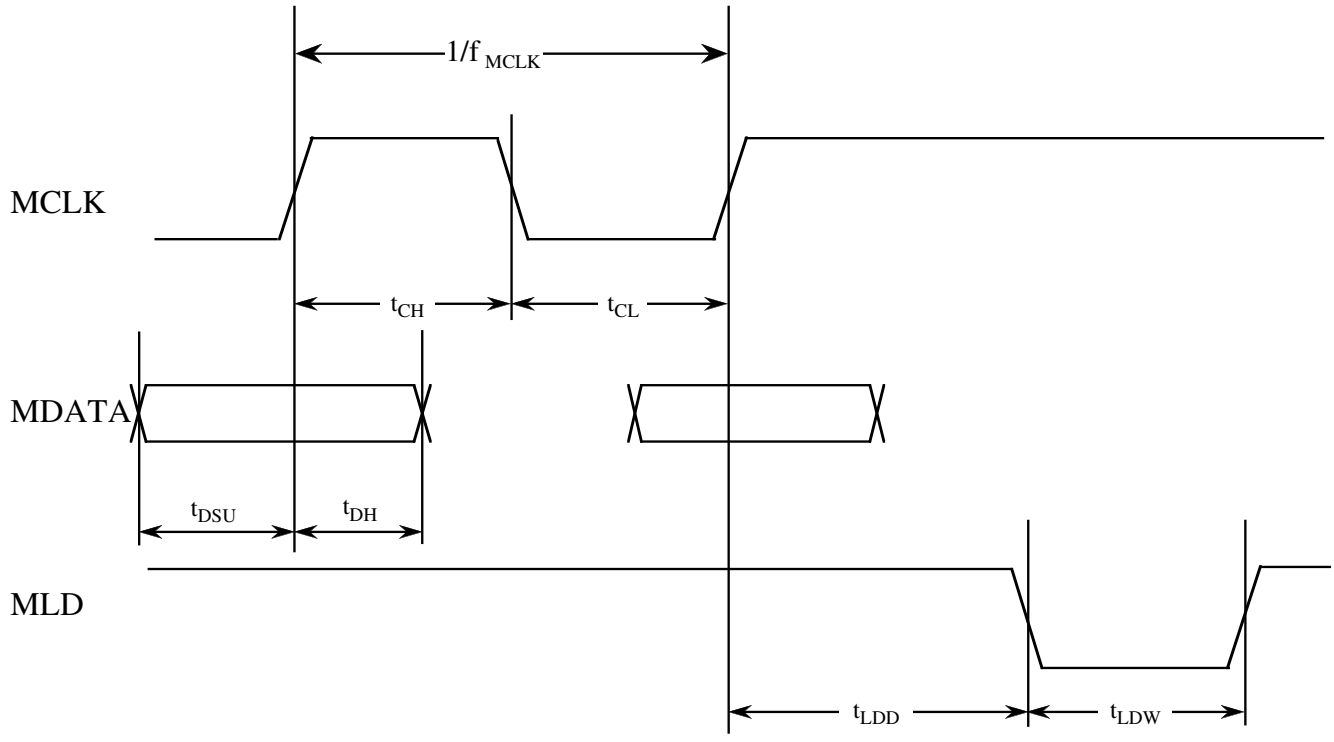






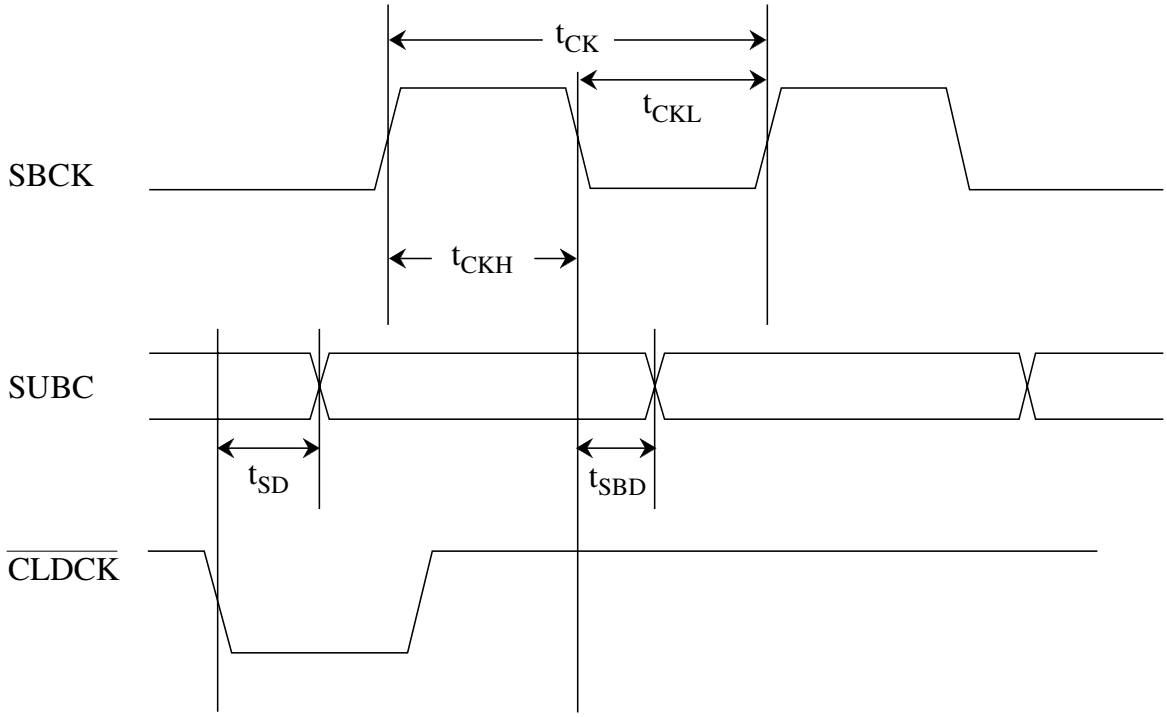
V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
Microcomputer Instruction Input Timing							
C74	Clock frequency	f_{MCLK}				1	MHz
C75	Clock pulse width	t_{CH}, t_{CL}		300			ns
C76	Data setup time	t_{DSU}		300			ns
C77	Data hold time	t_{DH}		300			ns
C78	Delay time	t_{LDD}		600			ns
C79	Latch pulse width	t_{LDW}		0.6		100	µs



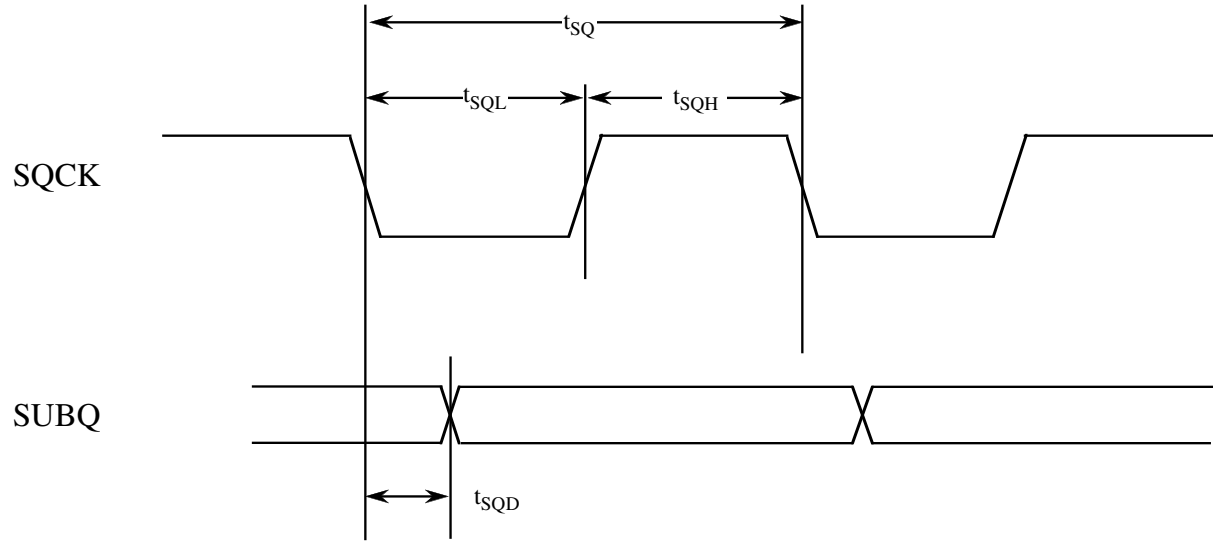
V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
Subcode Interface (1)							
C80	Clock width	t_{CK}		1			µs
C81	High-level pulse width	t_{CKH}		400			ns
C82	Low-level pulse width	t_{CKL}		400			ns
C83	Delay time	t_{SBD}				300	ns
C84	Setup delay time	t_{SD}				300	ns



V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

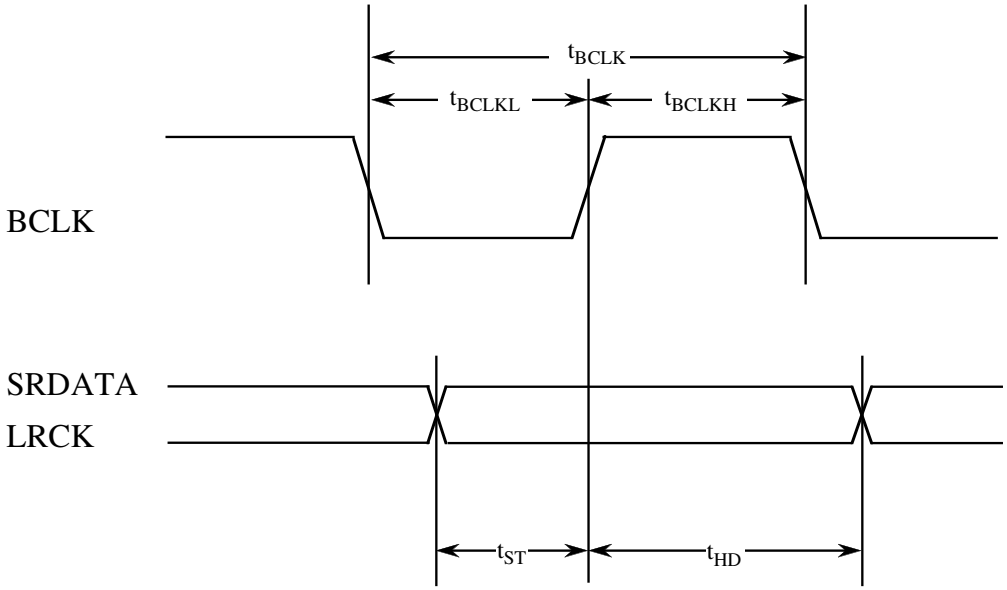
Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
Subcode Interface (2)							
C85	Clock width	t_{SQ}		500			ns
C86	High-level pulse width	t_{SQH}		200			ns
C87	Low-level pulse width	t_{SQL}		200			ns
C88	Delay time	t_{SQD}				150	ns



V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

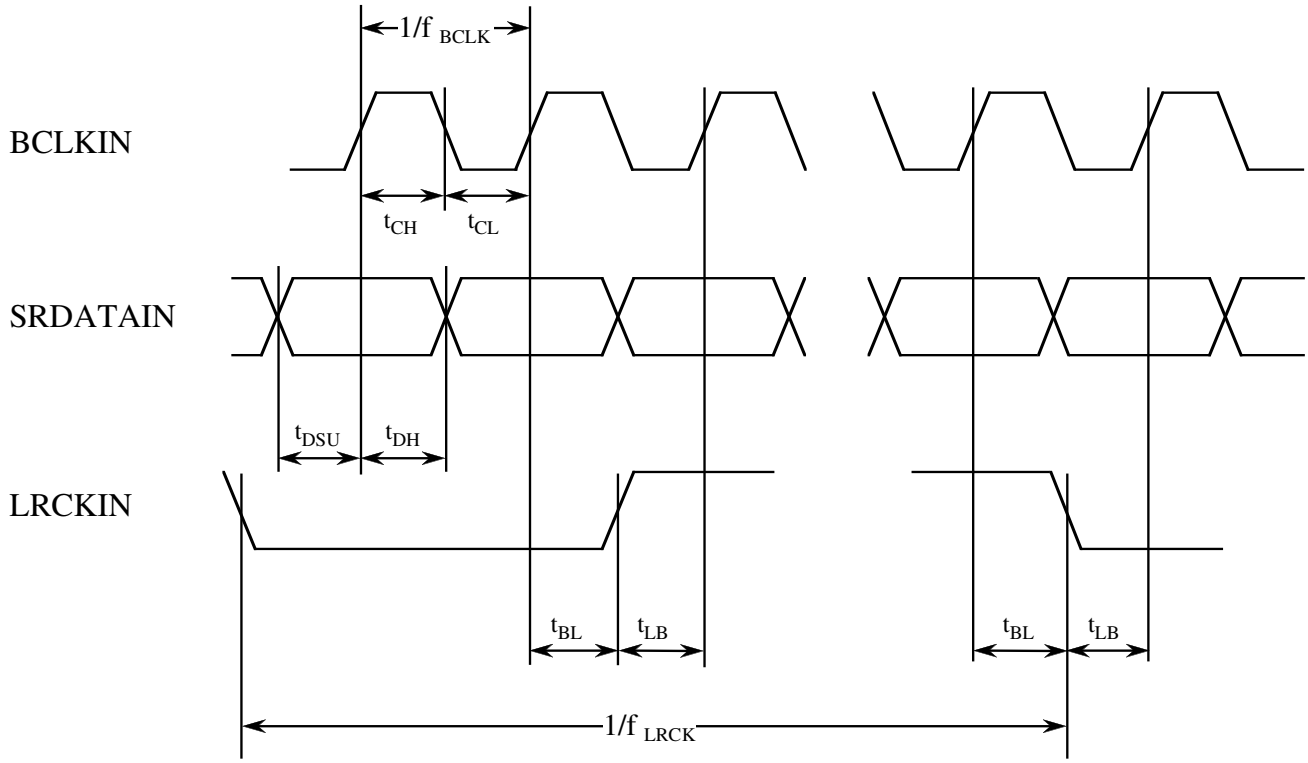
	Parameter	Symbol	Conditions	Limits			Unit
				min	typ	max	
	D/A Output Interface 1 ＊5						
C89	Clock width	t_{BCLK}	Normal-speed playback mode		354		ns
C90	High-level pulse width	t_{BCLKH}			177		ns
C91	Low-level pulse width	t_{BCLKL}			177		ns
C92	Setup time	t_{ST}		70			ns
C93	Hold time	t_{HD}		70			ns
	D/A Output Interface 2 ＊5						
C94	Clock width	t_{BCLK}	2x-speed playback mode		177		ns
C95	High-level pulse width	t_{BCLKH}			88.5		ns
C96	Low-level pulse width	t_{BCLKL}			88.5		ns
C97	Setup time	t_{ST}		30			ns
C98	Hold time	t_{HD}		30			ns
	D/A Output Interface 3 ＊5						
C99	Clock width	t_{BCLK}	4x-speed playback mode		88.5		ns
C100	High-level pulse width	t_{BCLKH}			44.2		ns
C101	Low-level pulse width	t_{BCLKL}			44.2		ns
C102	Setup time	t_{ST}		15			ns
C103	Hold time	t_{HD}		15			ns

＊5
D/A Output Interface



V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

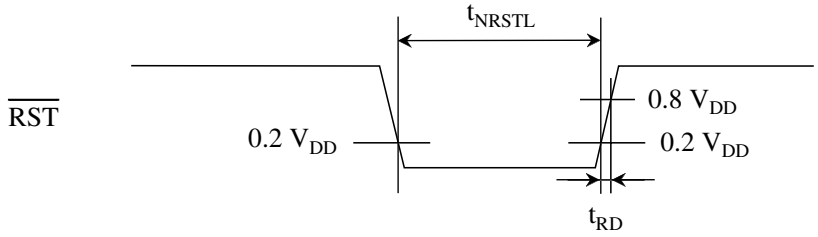
Parameter	Symbol	Conditions	Limits			Unit
			min	typ	max	
D/A Converter Input Timing						
C104 BCLK frequency	f_{BCLK}				4	MHz
C105 BCLK pulse width	t_{CH}, t_{CL}		70			ns
C106 Data setup time	t_{DSU}		70			ns
C107 Data hold time	t_{DH}		70			ns
C108 LRCK frequency	f_{LRCK}			44.1		kHz
C109 BCLK-LRCK timing	t_{BL}, t_{LB}		70			ns



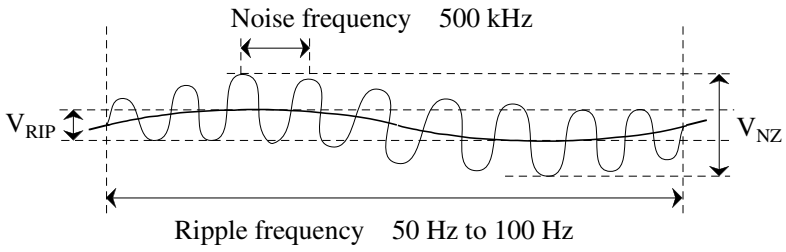
V_{CC5V}=5.0 V
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−30 ℃ to +85 ℃
f_{X1}=16.9344 MHz or 33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				min	typ	max	
Reset Timing (Note 19)							
C110	$\overline{RST}$ pulse width	t_{NRSTL}		200			μs
C111	Rise time	t_{RD}				100	ns
Power Supply Ripple Noise (Note 20)							
C112	Ripple amplitude	V_{RIP}				15	mV[P-P]
C113	Ripple noise amplitude	V_{NZ}				50	mV[P-P]

Note 19) When the power is turned on, reset with the $\overline{RST}$ pulse which is equal to or exceeds the above pulse width only after the clock oscillation is stabilized within ±10 % of error of the specified oscillation frequency.

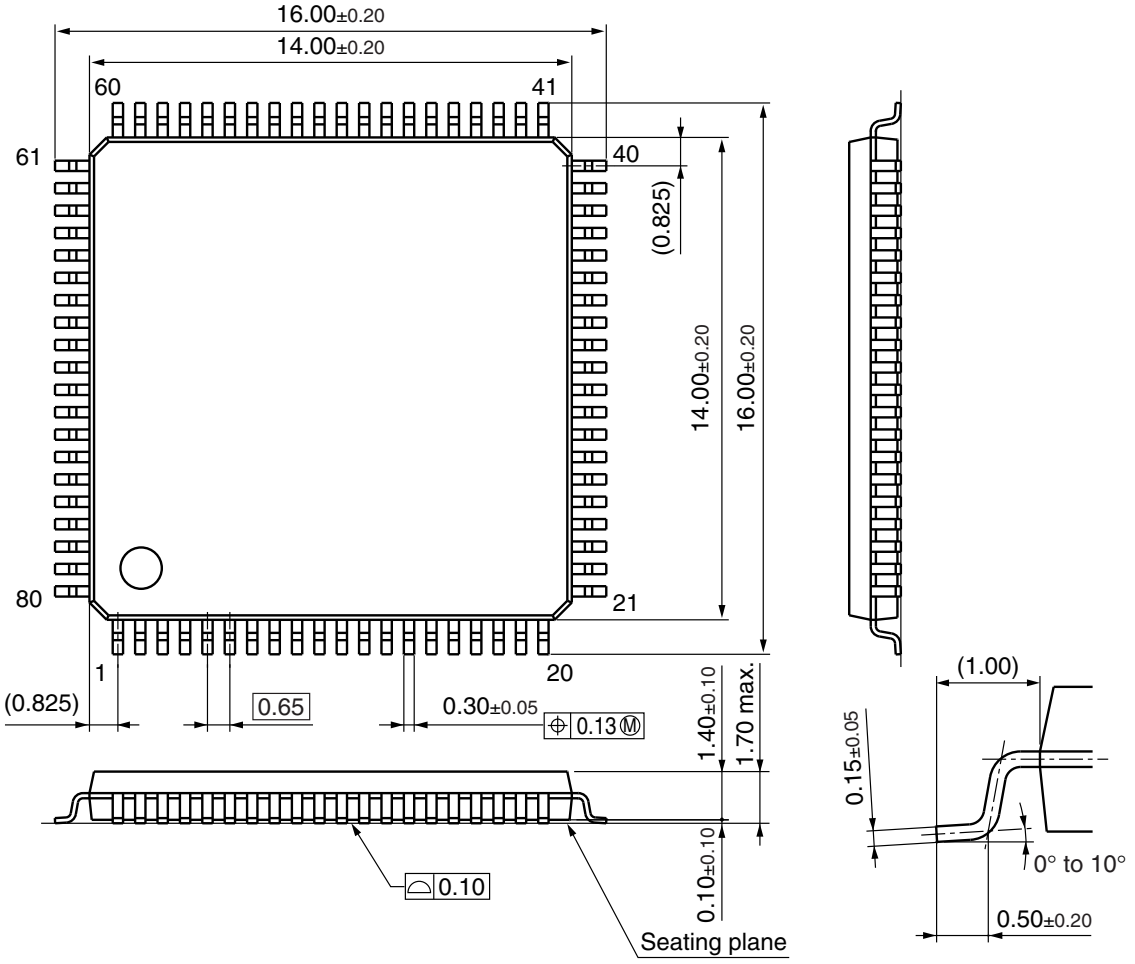


Note 20) The standard ripple noise values of the LSI are guaranteed on condition that the values apply to typical 50-Hz to 100-Hz ripples with 500-kHz typical noise and that both the ripples and noise are in sine waveform as shown below.
The values, however, vary under the influence of other parts located on the PCB. Therefore, be sure to check the actual values before applying the LSI to practical applications.



Package Dimensions (Unit: mm)

• LQFP080-P-1414A (lead-free package)



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(6) When designing your equipment, comply with the guaranteed values, in particular those of maximum rating, the range of operating power supply voltage, and heat radiation characteristics. Otherwise, we will not be liable for any defect which may arise later in your equipment.
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