LA5632



Multiple Power Supply System Regulator

Overview

The LA5632 is a multiple power supply IC that provides two 3.3-V regulator circuits as well as two 5-V regulator circuits. This device is optimal for MD players and similar applications.

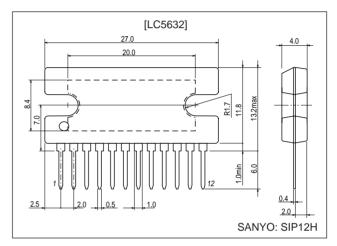
Functions and Features

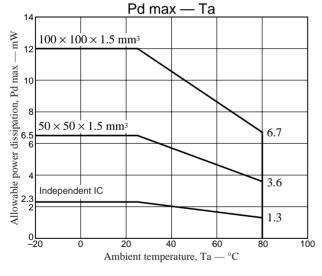
- Two built-in 3.3-V regulator circuits ($I_0 = 60 \text{ mA}$, 150 mA)
- Two built-in 5-V regulator circuits ($I_0 = 1000 \text{ mA}$, 100 mA)
- Power on/off detection circuit included
- The reset circuit operates from the B.BAK voltage.
- The reset circuit current drain is extremely low (3.5 μA (typical) in backup mode)

Package Dimensions

unit: mm

3149A-SIP12H





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Specifications Maximum Ratings at $Ta = 25^{\circ}C$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|----------------|-------------|------|
| Input voltage | V _{CC} max | | 14 | V |
| AC input voltage | AC max | | 2 | V |
| Allowable power dissipation | Pd max | Independent IC | 2.3 | W |
| Operating temperature | Topr | | -20 to +80 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

Operating Conditions at $Ta = 25^{\circ}C$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|------------|------------|------|
| Input voltage | V _{CC} | | 6.25 to 12 | V |
| Reset circuit input voltage | V _{B.BAK} | | 1.4 to 3.5 | V |
| PH5 output current | I _{PH5} | | 0 to 1000 | mA |
| B.BAK output current | I _{B.BAK} | | 0 to 60 | mA |
| ANA5 output current | I _{ANA5} | | 0 to 100 | mA |
| SYS3.3 output current | I _{SYS3.3} | | 0 to 150 | mA |
| S.RESET sink current | I _{SINKS} | | 0 to 0.2 | mA |
| P.DOWN sink current | I _{SINKP} | | 0 to 1 | mA |
| AC input current | I _{AC} | | 0 to 1 | mA |

Electrical Characteristics at $Ta = 25^{\circ}C$

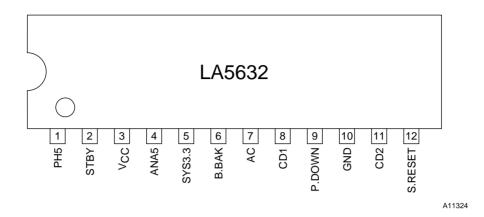
| Parameter | Querrale al | Conditions | Ratings | | | 1.1-14 |
|--|--------------------------|-----------------------------------|---------|------|------|--------|
| | Symbol | | min | typ | max | Unit |
| [PH5 Regulator Block] V _{CC} = 10 V, I _{PH5} = 1 | 000 mA | | | | | |
| Output voltage | V _O PH5 | | 4.75 | 5 | 5.25 | V |
| Dropout voltage | V _{DROP} PH5 | | | 0.5 | 1 | V |
| Line regulation | ΔV_{OLN} PH5 | V _{CC} = 6.25 to 12 V | | | 200 | mV |
| Load regulation | ΔV _{OLD} PH5 | I _{PH5} = 5 to 1000 mA | | | 200 | mV |
| Peak output current | I _{OP} PH5 | | 1000 | 1400 | | mA |
| Output shorted current | I _{OSC} PH5 | | | 400 | 1000 | mA |
| Current drain | I _Q PH5 | | | 70 | 112 | mA |
| [SYS3.3 Regulator Block] V _{CC} = 10 V, I _{SYS3} | _{3.3} = 150 mA | | | • | | |
| Output voltage | V _O SYS3.3 | | 3.13 | 3.3 | 3.47 | V |
| Dropout voltage | V _{DROP} SYS3.3 | | | 2 | 3.5 | V |
| Line regulation | ΔV _{OLN} SYS3.3 | $V_{CC} = 6.25$ to 12 V | | | 200 | mV |
| Load regulation | ΔV _{OLD} SYS3.3 | I _{SYS3.3} = 5 to 150 mA | | | 200 | mV |
| Peak output current | I _{OP} SYS3.3 | | 150 | 210 | | mA |
| Output shorted current | I _{OSC} SYS3.3 | | | 200 | 450 | mA |
| Current drain | I _Q SYS3.3 | | | 17.5 | 28 | mA |
| [ANA5 Regulator Block] V _{CC} = 10 V, I _{ANA5} = | = 1000 mA | • | | | | |
| Output voltage | V _O ANA5 | | 4.75 | 5 | 5.25 | V |
| Dropout voltage | V _{DROP} ANA5 | | | 0.5 | 1 | V |
| Line regulation | ΔV _{OLN} ANA5 | V _{CC} = 6.25 to 12 V | | | 200 | mV |
| Load regulation | ΔV_{OLD} ANA5 | I _{ANA5} = 5 to 100 mA | | | 200 | mV |
| Peak output current | I _{OP} ANA5 | | 100 | 140 | | mA |
| Output shorted current | I _{OSC} ANA5 | | | 40 | 100 | mA |
| Current drain | I _Q ANA5 | | | 17.5 | 28 | mA |
| Output noise voltage | V _{NO} ANA | 10 Hz ≤ f ≤ 100 kHz | | 120 | | μV |

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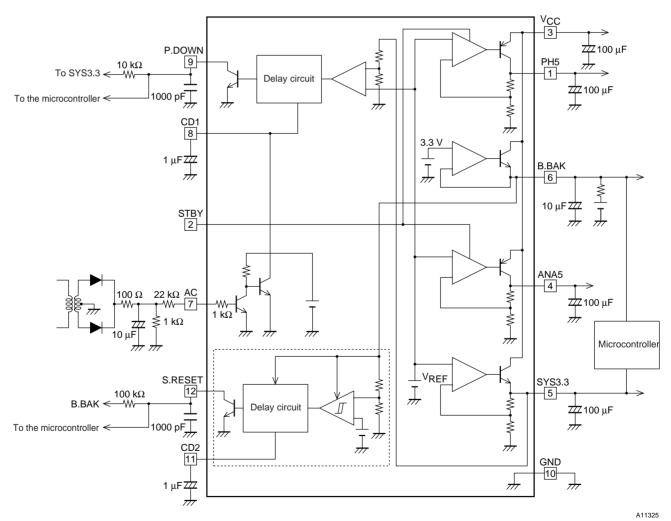
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| Demonster | Cumb ol | Conditions | | Ratings | | |
|--|---------------------------|--|---------|---------|------|------|
| Parameter | Symbol | | min | typ | max | Unit |
| [B.BAK Regulator Block] V_{CC} = 10 V, I _{BA} | _K = 60 mA | | | | | |
| Output voltage | V _O BAK | | 3.13 | 3.3 | 3.47 | V |
| Dropout voltage | V _{DROP} BAK | | | 2 | 2.5 | V |
| Line regulation | ΔV _{OLN} BAK | V _{CC} = 6.25 to 12 V | | | 200 | mV |
| Load regulation | ΔV_{OLD} BAK | $I_{BAK} = 5 \text{ to } 60 \text{ mA}$ | | | 200 | mV |
| Peak output current | I _{OP} BAK | | 60 | 84 | | mA |
| Output shorted current | I _{OSC} BAK | | | 60 | 180 | mA |
| Current drain | I _Q BAK | | | 15 | 24 | mA |
| [P.DOWN Detection Circuit] V_{CC} = 10 V | | · | · · · · | | | |
| Threshold voltage | V _{TH} P.DOWN | | 3.0 | 3.16 | 3.32 | V |
| Residual voltage | Vsat P.DOWN | With the cd1 pin shorted P.DOWN pin current = 1 mA | | | 200 | mV |
| Delay time | td1 | cd1 = 1 µF | 75 | 100 | 125 | ms |
| [S.RESET Block] V _{CC} = 0 V, B.BAK = 3.3 | 3 V | | | | | |
| Threshold voltage1 | V _{TH} 1 S.RESET | | 2.56 | 2.7 | 2.84 | V |
| Threshold voltage2 | V _{TH} 2 S.RESET | | 1.9 | 2.0 | 2.1 | V |
| Reset output undefined voltage | V _{UNS} S.RESET | | | | 1.4 | |
| Backup mode current drain | I _{IN} 1 BAK | B.BAK = 3.1 V | | 3.5 | 5 | μA |
| Low-level output current drain | I _{IN} 2 BAK | B.BAK = 1.8 V | | 0.36 | | mA |
| Residual voltage | Vsat S.RESET | With the cd2 pin shorted S.RESET pin current = 0.2 mA | | | 200 | mV |
| Delay time | td2 | cd2 = 1 µF | 75 | 100 | 125 | ms |
| [AC Detection Circuit] $V_{CC} = 10 V$ | | • | | | | |
| Threshold voltage | V _{TH} AC | | 0.5 | 0.7 | 0.9 | V |
| [STBY Detection Circuit] V _{CC} = 10 V | | • | | 1 | | |
| Threshold voltage | V _{TH} STBY | | 1.3 | 1.8 | 2.3 | V |

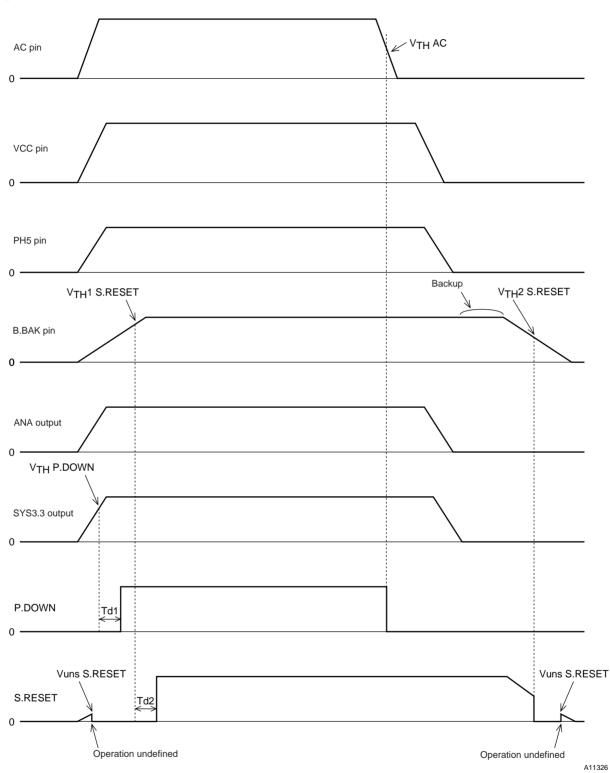
Pin Assignment



Block Diagram



Note: Use capacitors with low capacitance temperature coefficients for all capacitors.



Timing Chart

Note: The S.RESET output has an undefined operating state, so care is required in application design.

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