

OKI Semiconductor

MSM51V17400

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51V17400 is a new generation dynamic organized as 4,194,304-word × 4-bit. The technology used to fabricate the MSM51V17400 is OKI's CMOS silicon gate process technology. The device operates at a single 3.3V power supply. Its I/O pins are LVTTTL compatible.

FEATURES

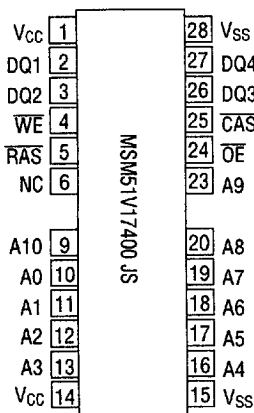
- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 4,194,304 word × 4-bit organization
- Single 3.3V power supply, ±10% tolerance
- Input: LVTTTL compatible
- Output: LVTTTL compatible, tristate
- Refresh: 2048 cycles/32ms
- Common I/O capability using "Early-Write" and "OE-Control-Write" operation
- Fast Page Mode, Read Modify Write capability
- \overline{CAS} before \overline{RAS} refresh, Hidden refresh, \overline{RAS} only refresh capability
- Multi bit test mode capability
- Package:
 - 28-Pin 400mil Plastic SOJ (SOJ28-P-400)
 - 28-Pin 400mil Plastic TSOP (TSOP28-P-400-K) (TSOP28-P-400-L)

PRODUCT FAMILY

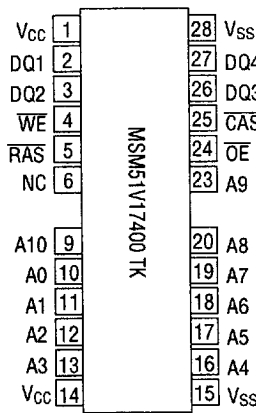
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM51V17400-60	60ns	30ns	15ns	15ns	110ns	432mW	1.8mW
MSM51V17400-70	70ns	35ns	20ns	20ns	130ns	396mW	
MSM51V17400-80	80ns	40ns	20ns	20ns	150ns	360mW	

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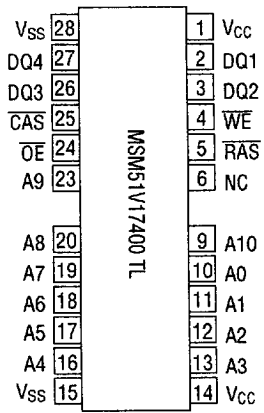
PIN CONFIGURATION (TOP VIEW)



28-PIN SOJ



28-PIN TSOP
(K TYPE)

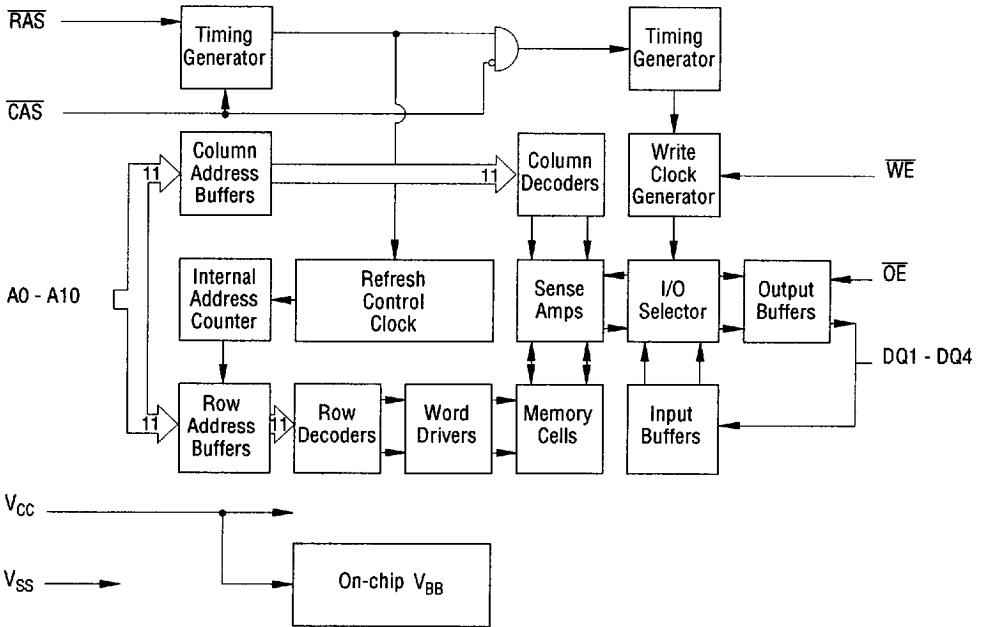


28-PIN TSOP
(L TYPE)

Pin Name	Function
A0 - A10	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
DQ1 - DQ4	Data-Input/Data-Output
OE	Output Enable
WE	Write Enable
V _{CC}	Power Supply (3.3V)
V _{SS}	Ground (0V)
NC	No Connection

Note: Same power supply voltage must be provided to every V_{CC} pin, and same GND voltage level must be provided to every V_{SS} pin.

FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-0.5 to 4.6	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	3.0	3.3	3.6	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

Capacitance

(V_{CC} = 3.0 to 3.6V, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	C _{IN1}	—	6	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ4)	C _{I/O}	—	10	pF

DC Characteristics

(V_{CC} = 3.0 to 3.6V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	MSM 51V17400-60		MSM 51V17400-70		MSM 51V17400-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	V _{OH}	I _{OH} = -2.0mA	2.4	V _{CC}	2.4		
Output Low Voltage	V _{OL}	I _{OL} = 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0V ≤ V _i ≤ V _{CC} +0.3V; All other pins not under test = 0V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQi = Disable 0V ≤ V _O ≤ 3.6V	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling t _{RC} = Min.	—	120	—	110	—	100	mA	1, 2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2V$	—	0.5	—	0.5	—	0.5		
Average Power Supply Current ($\overline{\text{RAS}}$ Only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling $\overline{\text{CAS}} = V_{IH}$ t _{RC} = Min.	—	120	—	110	—	100	mA	1, 2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{CAS}} = V_{IL}$ DQi = Enable	—	5	—	5	—	5	mA	1
Average Power Supply Current (CAS Before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}}$ cycling $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	120	—	110	—	100	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}} = V_{IL}$ $\overline{\text{CAS}}$ cycling t _{PC} = Min.	—	110	—	100	—	90	mA	1, 3

- Notes: 1. Specified values are obtained with the output open.
 2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

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AC Characteristics (1/2)


(V_{CC} = 3.0V to 3.6V, T_a = 0 to 70°C) Note 1, 2, 3, 10,11

Parameter	Symbol	MSM 51V17400-60		MSM 51V17400-70		MSM 51V17400-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t _{RMW}	155	—	185	—	205	—	ns	
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRMW}	85	—	100	—	105	—	ns	
Access Time from RAS	t _{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from CAS	t _{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from OE	t _{OEA}	—	15	—	20	—	20	ns	4
Access Time from CAS Precharge	t _{CPA}	—	35	—	40	—	45	ns	4
Output Low Impedance Time from CAS	t _{CLZ}	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	0	20	ns	7
OE to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	15	0	20	0	20	ns	7
Transition Time	t _r	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	
RAS Precharge Time	t _{RP}	40	—	50	—	60	—	ns	
RAS Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	100,000	70	100,000	80	100,000	ns	
RAS Hold Time	t _{RSH}	15	—	20	—	20	—	ns	
RAS Hold Time Reference to OE	t _{ROH}	10	—	10	—	10	—	ns	
CAS Precharge Time	t _{CP}	10	—	10	—	10	—	ns	
CAS Pulse Width	t _{CAS}	15	10,000	20	10,000	20	10,000	ns	
CAS Hold Time	t _{CSH}	60	—	70	—	80	—	ns	
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	ns	
RAS to CAS Delay Time	t _{RCD}	20	45	20	50	20	60	ns	5
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time from RAS	t _{AR}	50	—	55	—	60	—	ns	
Column Address to RAS Lead Time	t _{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V_{CC} = 3.0V to 3.6V, T_a = 0 to 70°C) Note 1, 2, 3, 10, 11

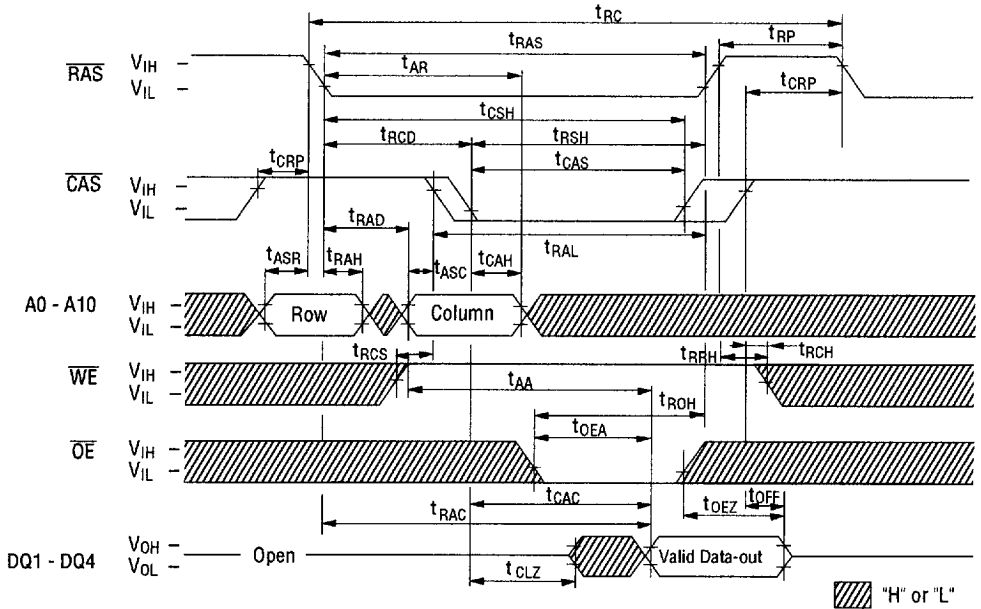
Parameter	Symbol	MSM 51V17400-60		MSM 51V17400-70		MSM 51V17400-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t _{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	45	—	55	—	60	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	15	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	12
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	ns	12
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	50	—	55	—	60	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OE D}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40	—	50	—	50	—	ms	9
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	55	—	65	—	70	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	85	—	100	—	110	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	60	—	70	—	75	—	ns	9
$\overline{\text{CAS}}$ Active Delay from $\overline{\text{RAS}}$ Precharge	t _{RPC}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t _{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t _{CHR}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t _{CPT}	40	—	40	—	40	—	ns	
$\overline{\text{We}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t _{WRP}	10	—	10	—	10	—	ns	
$\overline{\text{We}}$ Hold Time from ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$)	t _{WRH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t _{WSR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t _{WHR}	20	—	20	—	20	—	ns	


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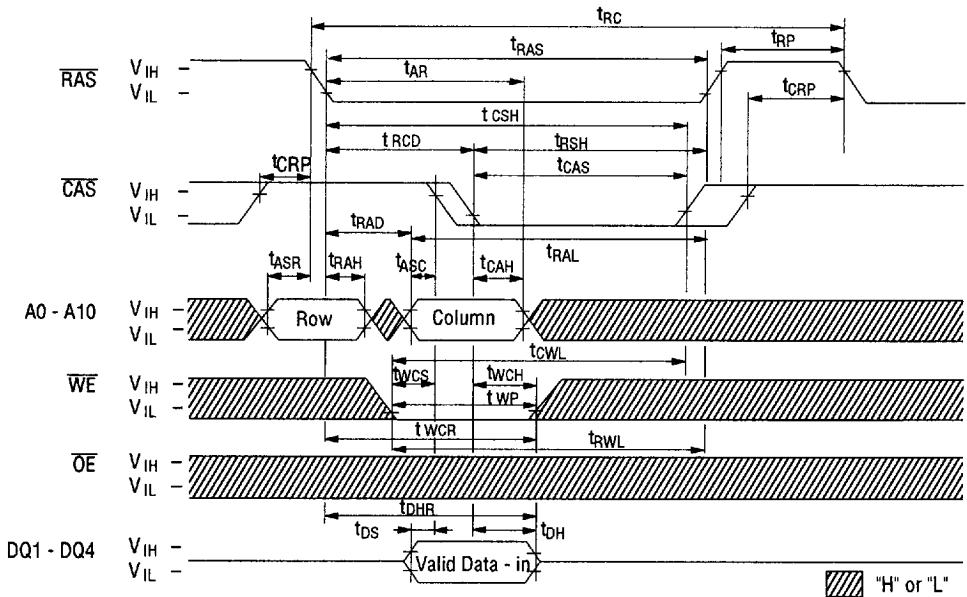
- Notes:
1. An initial pause of 200 μ s is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ initialization cycles is required.
 2. The AC characteristics assume $t_T = 5\text{ns}$.
 3. $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ are reference levels of input signals for timing measurement. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 1TTL loads and 100pF. Data Output timing reference levels are $V_{OH} = 2.0\text{V}$ and $V_{OL} = 0.8\text{V}$.
 5. Operation within the $t_{\text{RCD}}(\text{Max.})$ limit insures that $t_{\text{RAC}}(\text{Max.})$ can be met. $t_{\text{RCD}}(\text{Max.})$ is specified as a reference point only; If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{Max.})$ limit, then access time is controlled by t_{CAC} .
 6. Operation within the $t_{\text{RAD}}(\text{Max.})$ limit insures that $t_{\text{RAC}}(\text{Max.})$ can be met. $t_{\text{RAD}}(\text{Max.})$ is specified as a reference point only; If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{Max.})$ limit, then access time is controlled by t_{AA} .
 7. $t_{\text{OFF}}(\text{Max.})$ and $t_{\text{OEZ}}(\text{Max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{Min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{Min.})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{Min.})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{Min.})$, and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{Min.})$, the cycle is a read modify write cycle and data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 10. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated. In a test mode CA0, CA1 and CA10 are not used and each I/O pin now accesses 8-bit locations. Since all 4I/O pins are used, a total of 32 data bits can be written in parallel into the memory array. In a read cycle, if 8 data bits are equal, the I/O pin will indicate a high level. If the 8 data bits are not equal, the I/O pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{\text{RAS}}$ only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 11. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to specified value in this data sheet.
 12. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a $\overline{\text{OE}}$ control write cycle or a read modify write cycle.

TIMING WAVEFORM

Read Cycle

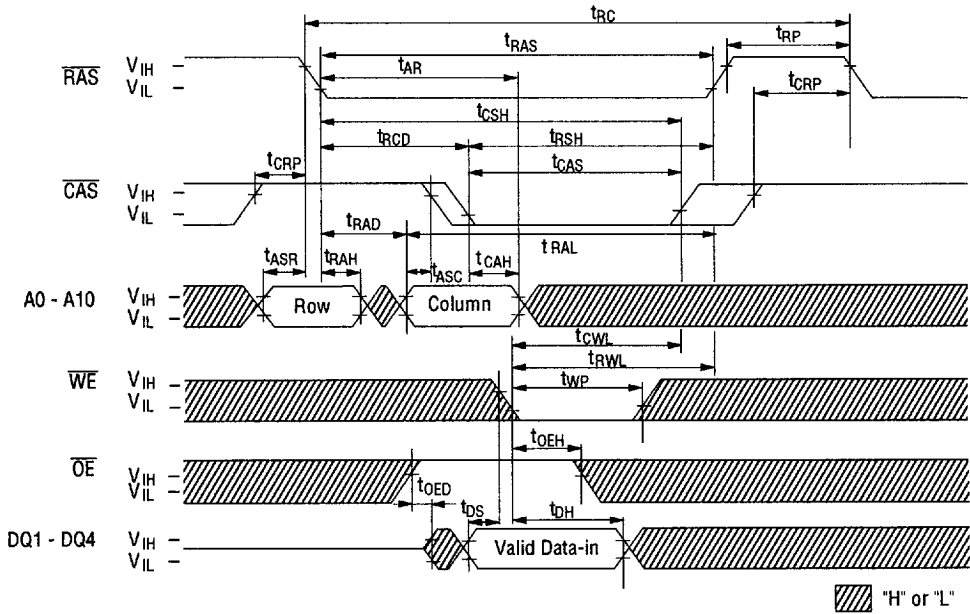


Write Cycle (Early Write)

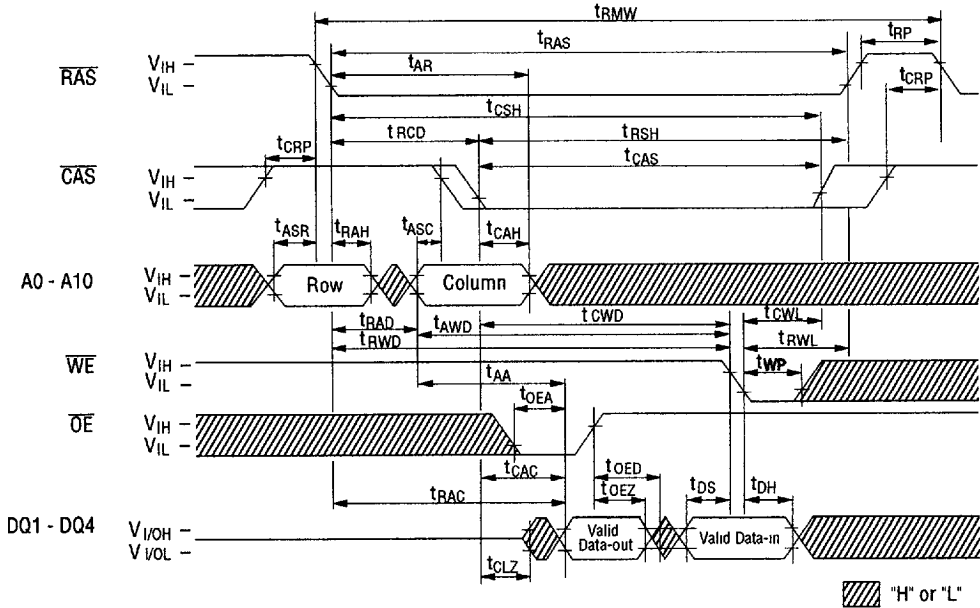


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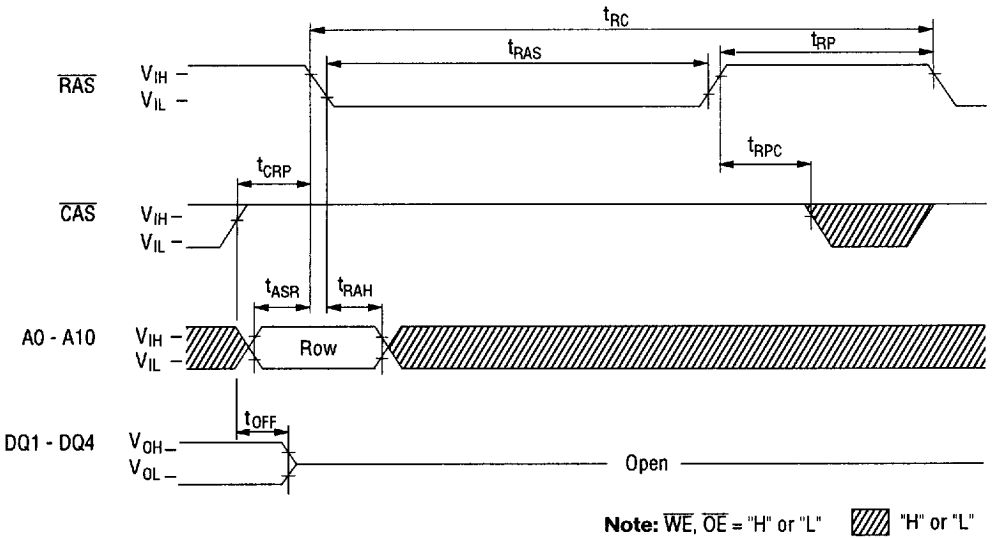
Write Cycle (OE Controlled Write)



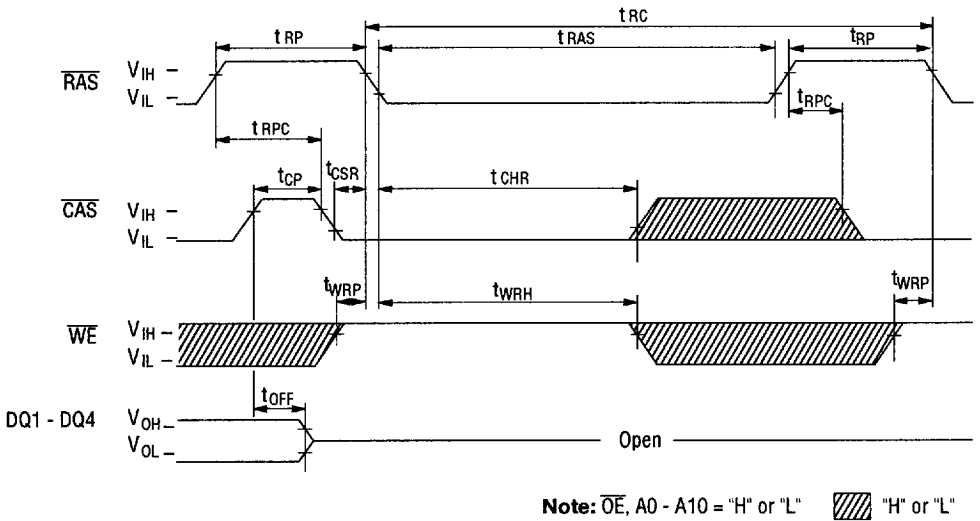
Read Modify Write Cycle



RAS Only Refresh Cycle

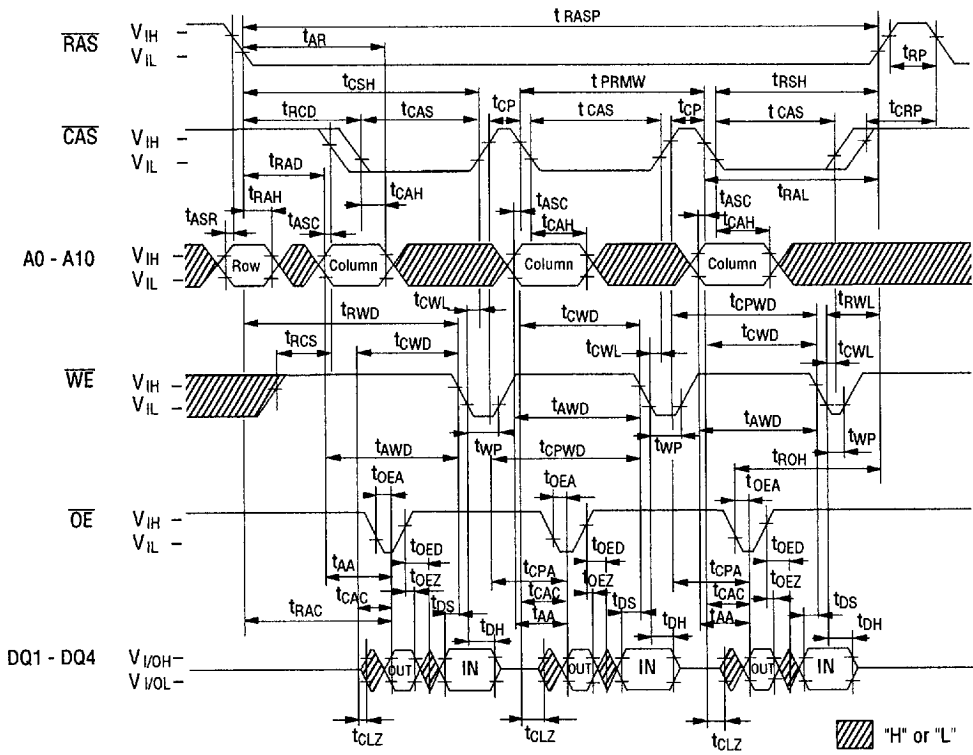


CAS Before RAS Refresh Cycle

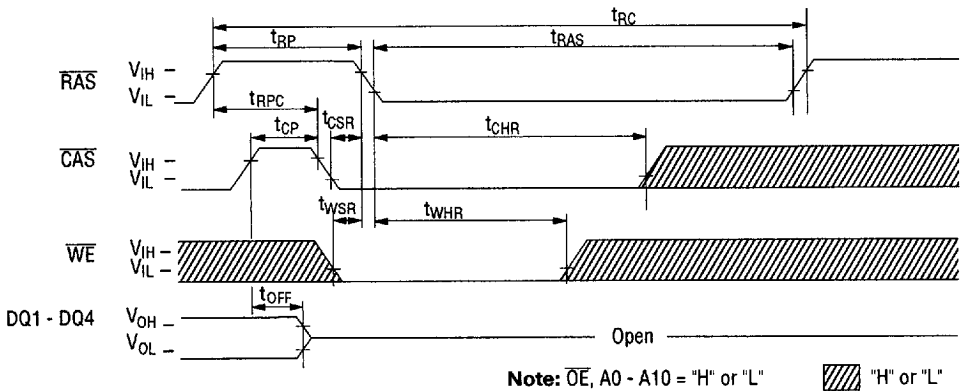


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Fast Page Mode Read Modify Write Cycle

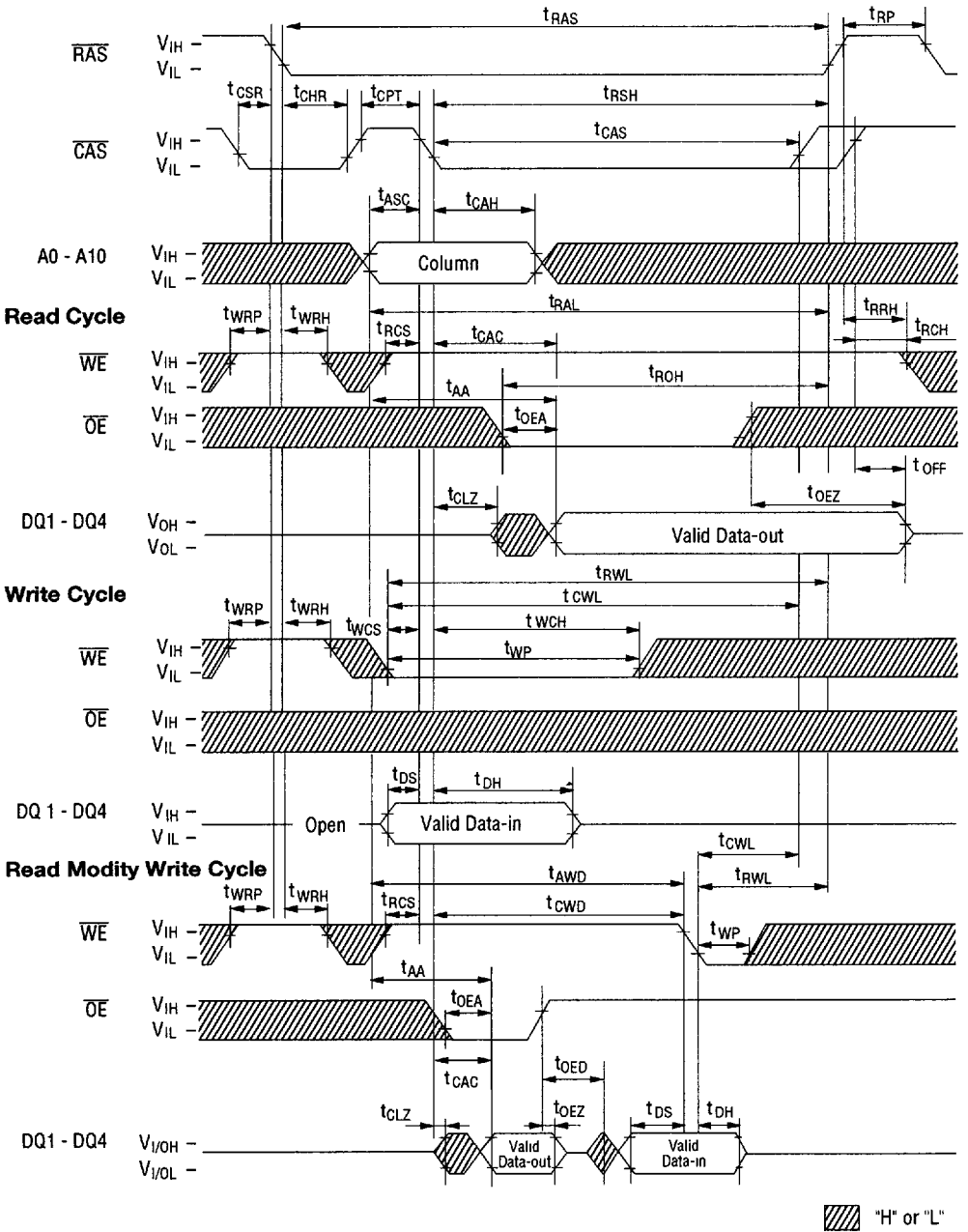


Test Mode in Cycle



Note: \overline{OE} , A0 - A10 = "H" or "L" "H" or "L"

CAS Before RAS Refresh Counter Test Cycle



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